CMOS IF-Baseband Processors for CDMA/FM Transceivers

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CDMA/FM 송수신기용 CMOS IF-Baseband 프로세서

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Abstract This paper describes CMOS IF-baseband processors for CDMA/FM applications. Processors consist of two chips, receiver and transmitter, respectively. The receiver includes the variable gain amplifier(VGA), quadrature mixers, low pass filters(LPFs), and analog-to-digital converters on a chip. The transmitter includes the DACs, LPFs, quadrature mixers, and the VGA capable of driving 1 dBm output power on a chip. A dB-linear variable gain amplifier is implemented using a parasitic PN diode in a CMOS process. Its characteristics offer high gain control dynamic range 90 dB, high linearity, good temperature characteristics and low power consumption. These processors are implemented in a 0.35 μm double-poly-four-metal CMOS silicon process with 25 GHz NMOS.

1. INTRODUCTION

Wireless phone designers face increasing pressure to develop smaller, lighter, and less expensive phones that provide longer talking and standby times. Therefore, semiconductor devices with high integration levels and low power consumption are needed[1]. Recently, transceivers using a CMOS process have been introduced. This paper describes two chips CDMA transceiver ICs. These chips use a single 2.7-3.5 V supply, achieve at least 250 MHz in the receiver and 150 MHz in the transmitter. The block diagram of a typical mobile phone system is shown in Fig.1. These chips interface between the radio frequency section and the digital part of the telephone system. The receiver circuit functions primarily convert analog IF signals to baseband frequency range and convert analog baseband signals into digital signals. The transmitter circuit transforms digital signals
into analog baseband signals which are up-converted to the IF frequency range.

![Fig. 1. Block diagram of a typical mobile unit.](image)

In the CDMA transceiver, variable gain amplifiers are needed for both receiver and transmitter automatic gain control. A transmit VGA is needed to regulate each mobile unit transmit power so equal power from each user is received at base station to optimize system performance.[1] The realization of VGA with 90 dB dynamic range is in a 0.35 um CMOS process. The gain control block of VGA for gain in dB linear function uses a parasitic PN diode in CMOS. This paper first explains the system architecture and block level descriptions. The transistor level circuit design of the VGA is then discussed. Finally, the performance of processors is presented.

II. RECEIVE PATH

The receiver section as shown in Fig.2 consists of Rx VGA, quadrature demodulator, low pass filters, A/D converters, clock synthesis, and mode control logic. To reduce the cross talk between signals and the effect of substrate noise, a receive signal path is designed to accept full differential signal with extending ±630 KHz from the IF center frequency. The 220.38 MHz received signal from the RF part is first amplified or attenuated by the Rx VGA to provide a constant amplitude signal to the quadrature demodulator. The gain of the VGA with 90 dB dynamic range is controlled by external voltage. The output of the VGA is separated into I-channel and Q-channel baseband components and then is fed to the quadrature mixer to be converted to baseband signal.

![Fig. 2. Functional block diagram of the receiver.](image)

This type of quadrature demodulator uses a double balanced architecture to reduce even harmonic components of the mixer. The quadrature demodulator must split the IF input into I/Q baseband signals with sufficient amplitude and phase accuracy. The gain is obtained in the down-conversion mixers while phase and amplitude accuracy is determined.
by the precision of the 90° phase shifter. The phase shifter has been realized using the digital divider. A 440.76 MHz differential signal is applied to two delay flip-flops in opposite polarity, so that the 220.38 MHz outputs from the flip-flops are out of phase by a 1/4 period. These outputs are used as LO signals to drive the down conversion mixers of the I/Q paths directly [35]. To reduce the DC offset voltage of signal paths and to improve matching, longer devices than the minimum size have been used.

The down-converted baseband signal is fed to filters. The Gm-C 7th order Elliptic filters for CDMA mode were chosen to suppress out-of-band signals, LO feed through and adjacent-channel interference. For FM mode, the 5 th order Elliptic filter was used. These filters are optimized for precise frequency response and filter flatness. Common mode feedback is used to achieve differential signal stability.

In the CDMA mode, analog I and Q baseband signals are converted to digital signals by the two 4-bit flash ADCs. The CDMA ADCs output a new 4-bit parallel digital value on each rising edge of the ADCs synchronous clock input signal. The ADC clock frequency of 9.8304 MHz is generated in the clock synthesis by dividing the 19.68 MHz system crystal oscillator frequency. The ADCs employ offset cancellation circuits. The DC offset is one of major problems in ADCs because the DC offset is superimposed on the wanted signal in the baseband.

The Rx signal path for FM looks quite similar to that of the CDMA as shown in Fig.2. Only the I/Q low pass filters and the ADCs are different. The IF center frequency is 85.38MHz and the modulation extends within ±12.2 KHz. Offset control for FM ADCs is similar to that of CDMA ADCs. In the FM, I signal and Q signal are quantized into an 8-bit digital word in the algorithmic ADCs with serial output.

III. TRANSMIT PATH

As shown in Fig.3, the Tx signal path has similar blocks to the Rx path. It interfaces between the modem and RF part, accepts 8-bit I/Q transmit data and outputs modulated signals, centered at 130.38 MHz. Eight bits of I and Q Tx data are input to the CDMA DACs using current scaling architecture. Each DAC is followed by low pass filters with 630 KHz bandwidth to remove unwanted frequency components. The filtered I and Q analog signals are each mixed into the quadrature modulator with I/Q LO at 130.38
MHz. Their outputs are summed and fed to the Tx VGA. Depending on external voltage, the Tx VGA varies in output power from a minimum of 83 dBm to a maximum of 0 dBm.

The Tx VCO has the same architecture as the Rx VCO, except that the VCO frequency is centered at 260.76 MHz and tuned by an internal PLL. An 8-bit algorithmic ADC is employed in monitoring the analog functions of subscriber unit such as battery level, temperature, and RF output power level.

Fig. 4. Simplified circuit diagram of the VTA.

**IV. VGA DESIGN**

It is necessary for the VGA to have the following properties: 1) Low noise figure; 2) Gain in a dB linear function of control voltage and a minimum gain control range of 90 dB; 4) Low power supply\cite{4}. To meet the system requirements, the input stage of the preamplifier in the Rx VGA uses a resistive shunt feedback architecture\cite{4}, gain control is distributed in each VTA, and a parasitic PN diode is chosen to achieve exponential function.

Variations in the gain of a VGA, built in a CMOS process, can be obtained by either varying the transconductance of a MOS device operated in the saturation region or varying the drain-source voltage Vds of a MOS device in the linear region. The transconductance of a MOS in the saturation region varies as the square root of the bias current. That method entails a lot of power dissipation to obtain gain variation. However, that of a MOS in the linear region is proportional to Vds and so does not have this drawback. The Tx VGA has been split into six stages. The VTA has low output swing but has high gain dynamic range.

Fig. 5. Exponential function circuit.

The last stage amplifier of the VGA has a constant gain of 20 dB. A simplified schematic of a two-input differential VTA is shown in Fig. 4. It consists of NMOS M1-M4 biased by PMOS M6-M7. Transistors M1 and M2 operate in the triode region with Vds and Vgs. The voltage Vds is set in the cascade transistors M3-M4. The full differential signals Vin+ and Vin− are applied to the gates in M1-M2 and
superimposed on the dc bias $V_{gs}$. The bias voltage $V_c$ of M4-M5 sets the value of $V_{ds}$ of M1-M2 and their transconductance value. It is straightforward to show that the equivalent transconductance $G_m$ of the VTA is given by

$$G_m = C_{ox} \left( \frac{W}{L} \right) V_{ds} \quad (1)$$

In this equation, $W$ = the channel width of M1-M2, $L$ = channel length of M1-M2. One important feature of this transconductance is its excellent linearity, which results in low distortion. Distortion is due to the $V_{ds}$ variations, and so a common mode feedback is chosen to reduce $V_{ds}$ variations.

Since $G_m$ is linearly proportional to $V_{ds}$, for gain in a dB linear an exponential gain control function is needed. A simplified block diagram of an exponential gain control circuit is shown in Fig. 5. Using a parasitic PN diode in a CMOS process, the output voltage $V_O$ of the VT generator is made to be a function of the external control $V_{ctrl}$, reference voltage $V_{ref}$ and thermal voltage $V_T$.

$$V_O = C \left( \frac{V_{ctrl}}{V_{ref}} \right) V_T \quad (2)$$

$$I_o = \exp \left( \frac{V_O}{V_T} \right) \quad (3)$$

$$V_c = R \exp \left( C \left( \frac{V_{ctrl}}{V_{ref}} \right) \right) \quad (4)$$

V. MEASUREMENTS

The IF processors described above were fabricated by 0.35 um CMOS technology with $f_T = 25$ GHz. The technology has poly resistors and poly-poly capacitors.

Interference is the major limiting factor in the performance of mobile systems. Sources of interference include other mobile in the same cell, a call in progress in a neighboring cell, and so on. The two major types of interference are co-channel interference and adjacent channel interference. To test the receivers immunity to the above interference as well as the spurious emission of the transmitter, two-tone tests were used. In the receivers test, a IIP3 of 1.6 dBm and a spurious content of 25 dBc as shown in Fig. 6 were obtained. In the transmitters test, a SFDR of 37 dBc was obtained.

![Graph](image)

Fig. 7. Measured gain characteristics of the Tx VGA versus external voltage.

Fig. 7 shows the gain characteristic of the Tx VGA versus external control voltage. Its linearity is 0.5 dBV. The gain error and phase...
Table 1. Measured key parameters of the receiver and transmitter.

<table>
<thead>
<tr>
<th>Receiver Chip</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>3.7 mm x 3.7 mm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.7 - 35 V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>22 mA</td>
</tr>
<tr>
<td>Minimum Input Power</td>
<td>-102 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>1.6 dBm</td>
</tr>
<tr>
<td>Spurious Content</td>
<td>-3.3 dBm</td>
</tr>
<tr>
<td>RSB</td>
<td>25</td>
</tr>
<tr>
<td>Transmitter Chip</td>
<td></td>
</tr>
<tr>
<td>Die Size</td>
<td>3.6 mm x 3.9 mm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.7 - 3.5 V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>27 mA</td>
</tr>
<tr>
<td>Maximum Output Power</td>
<td>1.0 dBm</td>
</tr>
<tr>
<td>Gain Slope Linearity</td>
<td>0.5 dBV</td>
</tr>
<tr>
<td>In-Band SFDR</td>
<td>37 dBc</td>
</tr>
<tr>
<td>I,Q Gain Mismatch</td>
<td>0.34 dB</td>
</tr>
<tr>
<td>I,Q Phase Imbalance</td>
<td>2 deg</td>
</tr>
</tbody>
</table>

error of I signal and Q signal in the receiver are 0.9 dB and 2.0 deg, respectively.

Total supply currents in the receiver and the transmitter are 22 mA and 27 mA, respectively, at 3V. The summary of the measured key parameters is shown in Table 1.

Fig. 8 shows a microphotograph of the receiver and Fig. 9 shows a microphotograph of the transmitter. The chip areas of the receiver and transmitter are 3.7 mm X 3.7 mm and 3.6 mm X 3.9 mm, respectively.

VI. CONCLUSION

The IF baseband processors for CDMA/FM have been designed using CMOS technology and successfully operating with a supply voltage of 2.7 to 3.5V. The VGA built in the IF-baseband processors has high gain control dynamic ranges and high linearity. To control the gain of the VGA, new circuits exploiting the use of a parasitic PN diode implementing a semi-logarithmic gain characteristic are described.

Fig. 8. Microphotograph of the receiver.

Fig. 9. Microphotograph of the transmitter.
REFERENCES


