Design of A 12-bit 100 MHz CMOS Digital-to-Analog Converter

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Abstract: In this paper, a 12-bit 100 MHz CMOS current steering digital-to-analog converter is designed. In the digital-to-analog converter, a driver circuit using a dynamic latch is implemented to obtain low glitch, a thermometer decoder is used for low DNL errors, guaranteed monotonicity, reduced glitching noise and a threshold voltage-compensated method current source is used. The digital-to-analog converter is designed with 0.35 μm CMOS technology at 3.3 V power supply and simulated by HSPICE.

1. Introduction

In the perspective of the recent research trend to fully integrated systems, the interface between the digital and the analog part of the system becomes one of the key building blocks in all communication systems. High speed and high resolution digital-to-analog converters enhance the performance of video systems, HDTV and wireless communications etc. For example, video digital-to-analog converters that are faster than 70 MHz and have more than 10-bit resolution are needed in HDTV applications [2]. In these applications, the CMOS digital-to-analog converter has the advantages of low power, low cost, easy integration and I/O compatibility with both TTL and external CMOS circuitry.

In this paper, a 12-bit 100 MHz CMOS current steering digital-to-analog converter is designed. Current steering digital-to-analog converter architectures are preferred to resistor string architectures. Because it has the advantages of high speed, high accuracy, short settling time, low power, and reduced chip size etc. But also it has the defects of mismatched switching time of the current cells and clock feed-through by the digital input signal and system input clock, which make the glitch noise and mismatched current between the switching current cells.

Therefore, in this digital-to-analog converter, a CMOS latch circuit is used for low switching glitch and a CMOS buffer is used for preventing clock feed-through. Also a driver circuit using a dynamic thermometer decoder is used for low DNL errors, guaranteed monotonicity, and reduced glitch noise and a threshold voltage-compensated method is used for stable current source [7]. The digital-to-analog converter is designed with 0.35 μm CMOS technology at 3.3 V power supply and simulated by HSPICE. The maximum power dissipation of the designed digital-to-analog converter is 143 mW. Figure 1 shows floor plan of the designed digital-to-analog converter.

2. The Thermometer-code Decoder

The architecture of the thermometer-code is not a minimal representation, but thermometer-code based converter does have advantages over the resistor string architecture. More importantly, a digital-to-analog converter based on a thermometer-code greatly minimizes glitches, as compared to binary-array approaches, since banks of resistors are never exchanged at slightly different times when the output should change by only 1 LSB. It is also of interest to note that the use of a thermometer code does not increase the size of the analog circuitry compared to a binary-weighted approach. The total area required by the transistor switches is the same since transistors are usually size-scaled in binary-weighted designs to account for the various current densities. All transistors switches in a thermometer-code approach are of equal sizes since they all pass equal currents.

In this paper, a trade-off between the achievable glitch and the complexity of the decoding logic has resulted in 4 binary weighted LSB’s, while the 8 (4+4) MSB’s are implemented in an unary weighted current source array. Figure 2 shows the whole block diagram of the designed 12-bit digital-to-analog converter. Figure 3 shows the designed 4-bit thermometer-code decoder circuit, which is used for each row and column decoder to select current cells by digital input signal. Figure 4 is the output of the 4-
bit thermometer-code decoder, which is simulated by HSPICE.

The main issue of the DAC is its very small glitch energy. In order to achieve this result, a number of problems have been solved. We must consider that the imperfect synchronization of the input signals at the gates of the current switches, the digital signal feed-through through the gate-drain capacitance from the current switches directly to the output, and the current variation due to a drain voltage variation of the current sources if both current switches are simultaneously in the off state [2]. These problems may be solved by using a latch circuit in front of the each switching current cell. The latch circuit is designed to operate by clock signal and two input signals which have opposite phase mutually for synchronization of the input of switching current cell.

In this paper, the latch circuit is added in front of the current switches to guarantee the synchronization of the input signals and three-MOS inverter is used for minimizing the clock feed-through and preventing both PMOS current switches are simultaneously in off state by decreasing inverter logic threshold and generating overlapped output waveforms. Figure 5 shows the designed latch circuit.

3. Design of The Latch and Buffer Circuit
Figure 7 is the output waveforms of the latch using the buffer of decreased inverter logic threshold.

Figure 7. Simulated output waveform of the latch

4. Design of The Current Source

For digital-to-analog converter using switched current cell, it is important to make output current of each cell same amount and stable. But, there is many factors which affect the output current on fabrication process. The threshold mismatch of each current cell is one of the number.

In this paper, threshold-voltage compensated current source is used for decreasing the mismatched current of each current cell by threshold mismatch on fabrication process, so that current source can be more stable and reduces glitch problems. Figure 8 is the designed switched current source which is added threshold-voltage compensated circuit.

![Figure 8. Threshold-voltage compensated switched current source](image)

The main transistors of the compensation circuit are $M_{14}$ and $M_{15}$. If we neglect the effective channel length modulation effect of $M_{11}$, then $I_{11}$ can be written as;

$$I_{11} = K \frac{W_{11}}{L_{11}} \left( V_{DD} - V_b - |V_{TH11}| \right)^2$$

where

$$\Delta V = V_{b2} - V_b - V_{TH14}$$

Figure 8 indicates that $V_{b2}$ and $I_b$ must be small for making $I_{11}$ more insensitive to the variation of threshold voltage. Besides, if $(W/L)_{15}$ is small and $I_b << I_{11}$ then $I_{11}$ is independent of $V_{TH11}$ and only function of $(W/L)_{11}$ like general MOS current equation [1].

Equation (2) indicates that $V_{b2}$ and $I_b$ must be small for making $I_{11}$ more insensitive to the variation of threshold voltage. Besides, if $(W/L)_{15}$ is small and $I_b << I_{11}$ then $I_{11}$ is independent of $V_{TH11}$ and only function of $(W/L)_{11}$ like general MOS current equation [1].

Figure 9 and 10 shows the output of a switched current cell which is consist of latch, inverter buffer and threshold-voltage compensated current source. Figure 9 is the output waveform of general inverter buffer and Figure 10 is the output waveform of three-MOS inverter buffer. The former case has about $\pm 50 \mu$A glitch current. The latter shows about $\pm 27 \mu$A glitch current and about $\pm 2$ mV glitch voltage for 75 $\Omega$ load.

![Figure 9. Output waveform of switched current cell using general inverter buffer](image)
5. Conclusion

In this paper, a digital-to-analog converter which has 12-bit resolution and 100 MHz operating clock is designed. The thermometer-code architecture and switched current source is used. We use latch circuit to synchronize the switched current inputs and use three-MOS inverter buffer to avoid clock feed-through and simultaneously off state of the both switching current inputs. Also threshold-voltage compensation circuit is added on the current cell for more stable current source. Designed digital-to-analog converter is simulated by HSPICE with 0.35 μm CMOS process at 3.3 V power supply and the maximum power dissipation is 143 mW.

References