# Sample/Holds, Voltage References, and Translinear Circuits

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## Sample and Holds

- A sample and hold is used to sample an analog signal and to store its value for length of time.
- Sample-and-hold circuits $\simeq$ track-and-hold circuits, except for a few switched-capacitor S/H circuits without tracking phase.
- S/H circuits can greatly minimize errors due to slightly different delay times in the internal operation of data converters.
- A *sampling pedestal* or a *hold step*: This error is the difference between the hold voltage and the input voltage at the time of sampling (track $\rightarrow$ hold). This error should be signal independent; otherwise it can introduce *nonlinear distortion*.



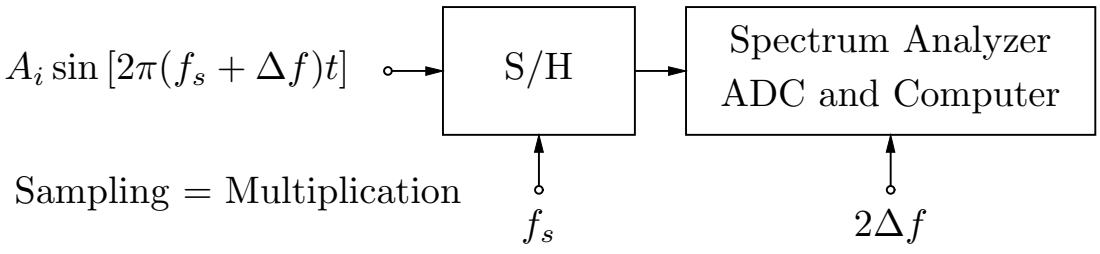
- The *signal isolation* between the input and the output of S/H circuits: In reality, there is always some signal feedthrough by parasitic capacitive coupling.
- The *speed* at which a S/H can track the input signal in sample mode. There are both small-signal and large-signal limitations due to 3-dB bandwidth and slew rate → *acquisition time* (hold → track).
- *Droop rate*: This error is a slow change in output voltage by leakage currents. In most CMOS designs, this can be ignored.
- *Aperture time* is delay time between hold command and real sample.
- *Aperture jitter* or *aperture time uncertainty*: the result of effective sampling time changing from one sampling instance to the next.
- Other parameters such as *dynamic range, linearity, gain*, PSRR, and *offset error* → design principles for minimizing these errors.





## A Popular Method for Testing S/Hs

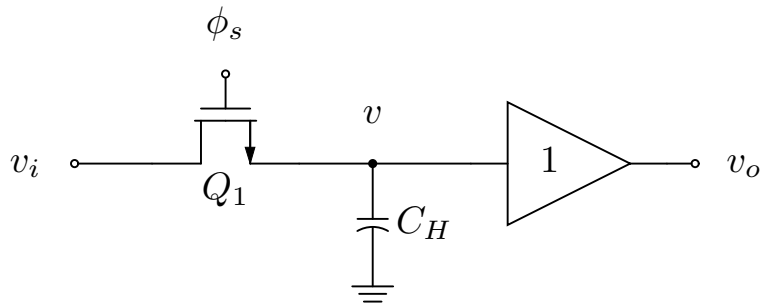
- *Beat test*: This test consists of clocking the S/H at its maximum clock frequency and applying a sinusoidal input signal whose frequency is *slightly* different from the clock frequency. The output is demodulated to a low (*beat*) frequency $\Delta f$ equal to the difference between the clock frequency and the signal frequency. This LF signal is then characterized by using a spectrum analyzer or by digitizing it using a high-accuracy ADC clocked at a frequency $\geq 2\Delta f$.






## MOS Sample-and-Holds Basics

❏ The simplest sample and hold: holding capacitor $C_H$.




❏ The charge injection: hold step $\Delta v \propto v_i$ (gain error), $V_{tn} = f(v_i)$ (signal-dependent error: distortion) ← body effect.

$$\Delta v = \frac{\Delta Q}{C_H} = -\frac{C_{ox}WLV_{\text{eff}}}{2C_H} = -\frac{C_{ox}WL(V_{DD} - V_{tn} - v_i)}{2C_H}$$

❏ The clock feedthrough: $\Delta v \neq f(v_i)$ (signal-independent offset),

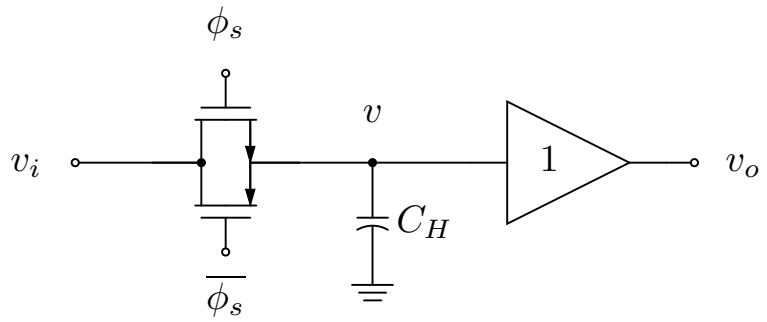




power-supply noise on clock signal (poor PSRR).

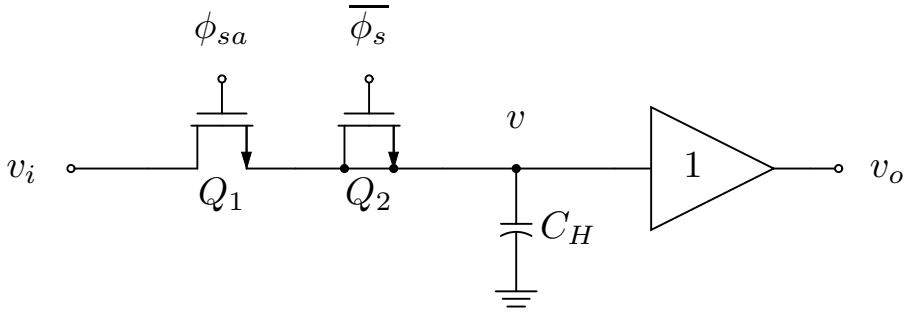
$$\Delta v = -\frac{C_{ox}WL_{ov}(V_{DD} - V_{SS})}{C_H}$$

❏ A track and hold with a CMOS transmission gate: same size, assuming $v_i$ in the middle region between $V_{DD}$ and $V_{SS}$ (same charges), fast and exactly complementary clock (same off times).

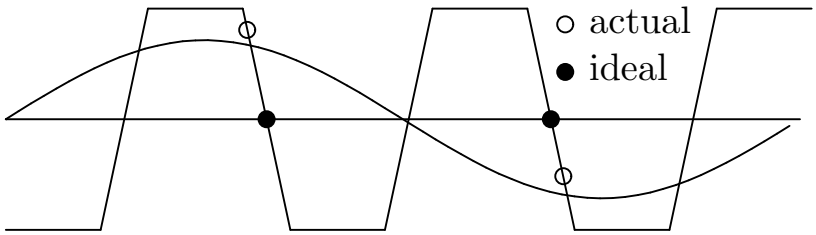



❏ A track and hold with a dummy switch: $W_2 = W_1/2$, fast clock waveform for good cancellation. The clock of $Q_2$ changes slightly

after that of $Q_1$ to guarantee that the charge of $Q_2$ cannot escape through $Q_1$. This technique can minimize $\Delta v$ to less than about 1/5




❏ Sampling jitter by clock waveforms having finite slopes: early, late.

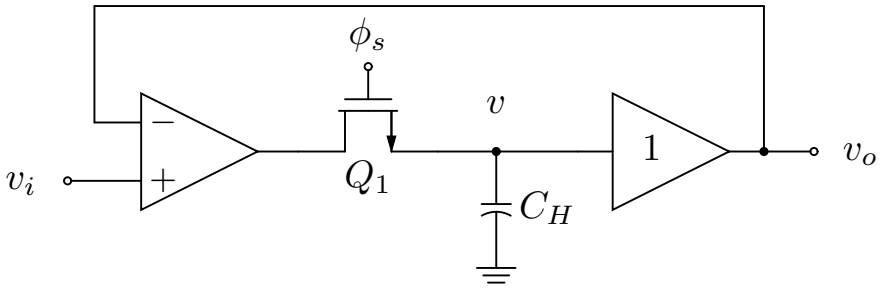







## A S/H Circuit with A Feedback Loop

❏ A S/H circuit including an opamp in a feedback loop: to increase $R_i$

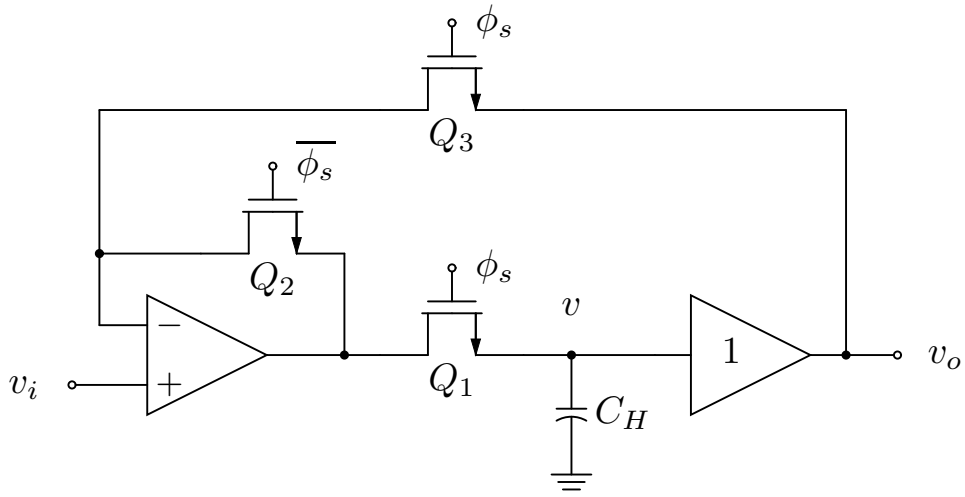



❏ $V_{OS}$ of the opamp will remain, but $V_{OS}$ of the buffer will not have an effect on $v_o = v_i + V_{OS}$. Errors due to charge injection, finite slopes.

❏ The speed can be seriously degraded due to frequency compensation. Another source of speed degradation is the slewing time it takes for the opamp to return from saturation (hold mode) to track mode.

## A S/H Circuit with Two Additional Switches

❏ A S/H circuit adding two switches to minimize slewing time.



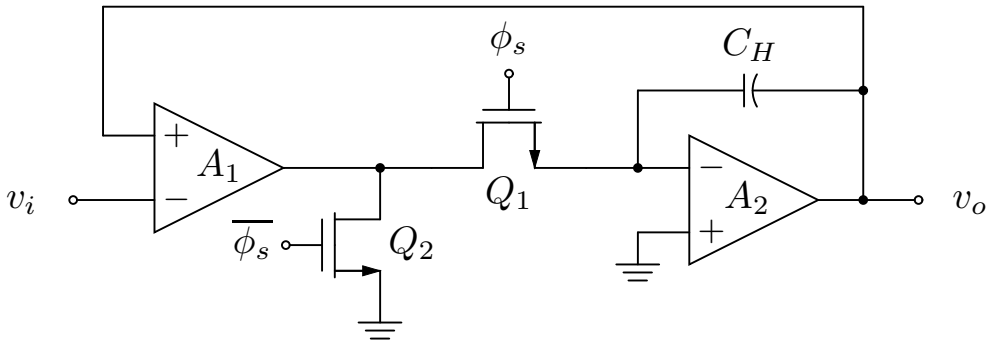

❏ This S/H still has errors due to charge injection from $Q_1$ and finite clock rise and fall times.





## An Improved S/H Circuit

❏ Signal independent error, slewing and signal feedthrough ↓ by $Q_2$, but speed ↓ due to frequency compensation of two opamps.

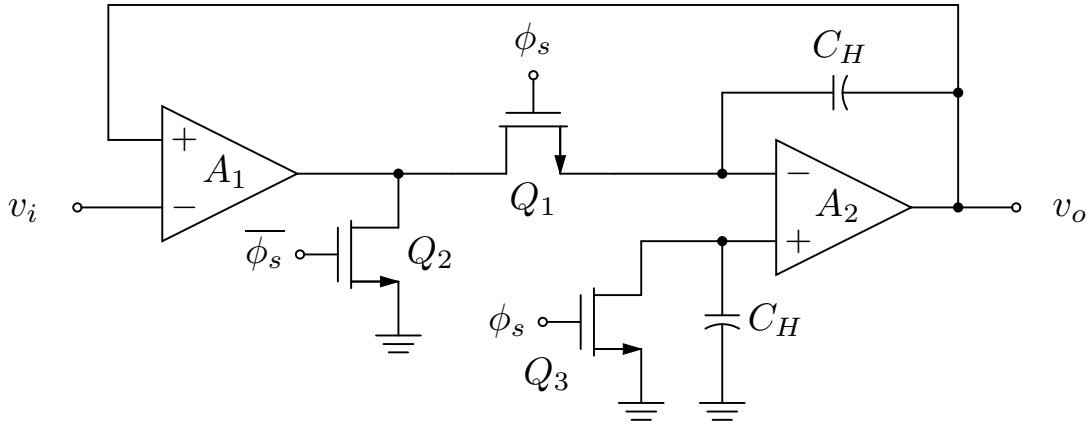



❏ The voltages on both sides of $Q_1$ are nearly signal independent as virtual ground. Thus the charge injection due to $Q_1$ will cause just a dc offset but no distortion. In addition, the sampling time will not change due to the finite slopes of clock waveform.



## A S/H with Clock-Feedthrough Cancellation

❏ A S/H circuit with additional circuitry to minimize the dc offset.




❏ The common-mode rejection of opamp will eliminate the effects of charge injection on the output voltage. This configuration using fully differential design is a reasonable choice for many applications.

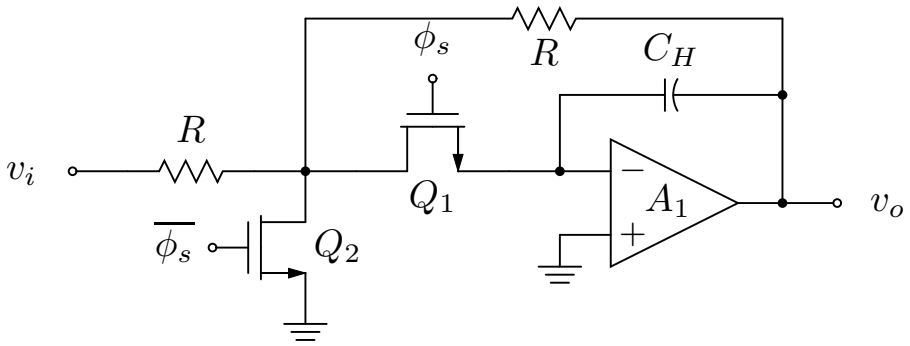




## Other Examples of CMOS S/H Circuits

❏ The choice for a S/H is dependent on application and technology.

❏ An inverting track and hold: clock feedthrough and sampling time are signal independent, track mode (LPF) $H(s) = -1/(1 + sRC_H)$.

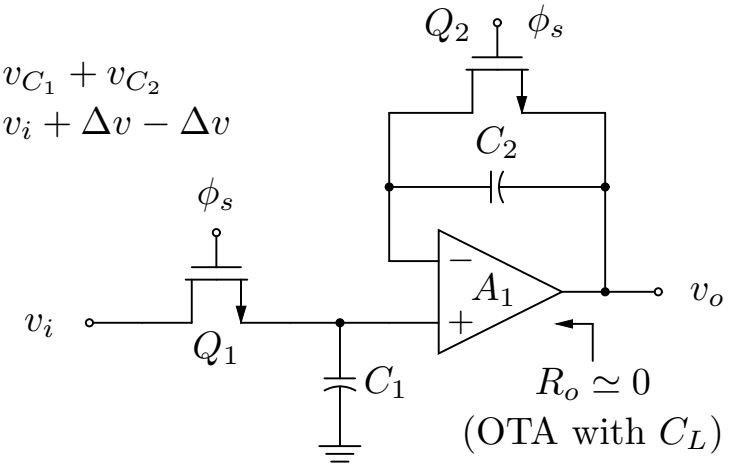



❏ A small capacitor $C_C$ can be included in parallel to the input resistor to improve the speed (APF) $\rightarrow H(s) = -(1 + sRC_C)/(1 + sRC_H)$.

## A S/H with Clock-Feedthrough Cancellation

❏ A simple noninverting S/H circuit for high-speed applications.

$$v_o = v_{C_1} + v_{C_2}$$
$$= v_i + \Delta v - \Delta v$$



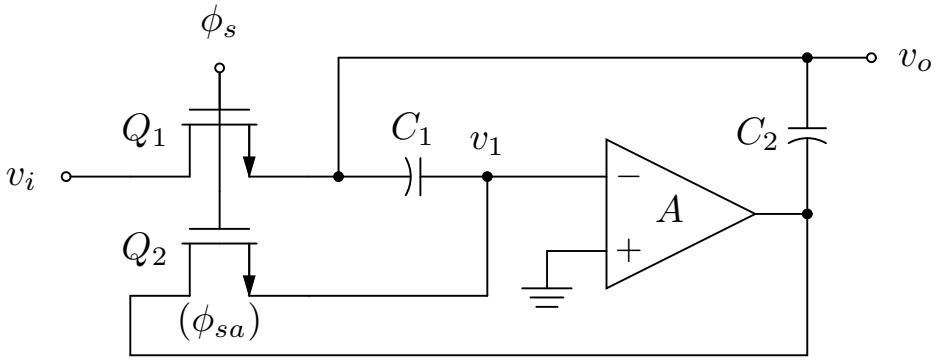

❏ The charge injection of $Q_1$ will be matched by the charge injection of $Q_2$ since both are at the same voltage and have the same clock.





## A S/H with Miller Holding Capacitor

❏ An open-loop S/H circuit with large Miller $C_H$: smaller capacitances, switches, and voltage changes at the output → very high speed.




❏ The effective holding capacitance at the inverting input of opamp.

$$C_H = (1 + A)C_1C_2/(C_1 + C_2)$$

❑ Reduction of charge injection error by Miller effect.

$$\Delta v_{o1} \simeq \Delta Q_1/AC_2, \quad \Delta v_{o2} \simeq \Delta Q_2/C_1 \text{ (dc offset)}$$

❑ Charge injection error by $Q_1$: $C_i$ = input capacitance of opamp.

$$\Delta Q_1 = \Delta Q_{C_1} + \Delta Q_{C_2}, \quad \Delta Q_{C_1} = \Delta Q_{C_i}$$

$$\Delta Q_{C_1} = (\Delta v_{o1} - \Delta v_1)C_1 = \Delta v_1 C_i, \quad \therefore \Delta v_1 = \frac{C_1 \Delta v_{o1}}{C_1 + C_i}$$

$$\Delta Q_{C_1} = \Delta v_1 C_i = \frac{C_i C_1}{C_1 + C_i}\Delta v_{o1}$$

$$\Delta Q_{C_2} = [\Delta v_{o1} - (-A\Delta v_1)]C_2 = \frac{(C_1 + C_i + AC_1)C_2}{C_1 + C_i}\Delta v_{o1}$$

$$\Delta Q_1 = \frac{(C_1 + C_2)C_i + (A+1)C_1C_2}{C_1 + C_i}\Delta v_{o1}$$

$$\Delta v_{o1} = \frac{(C_1 + C_i)\Delta Q_1}{(C_1 + C_2)C_i + (A+1)C_1C_2} \simeq \frac{\Delta Q_1}{AC_2}$$

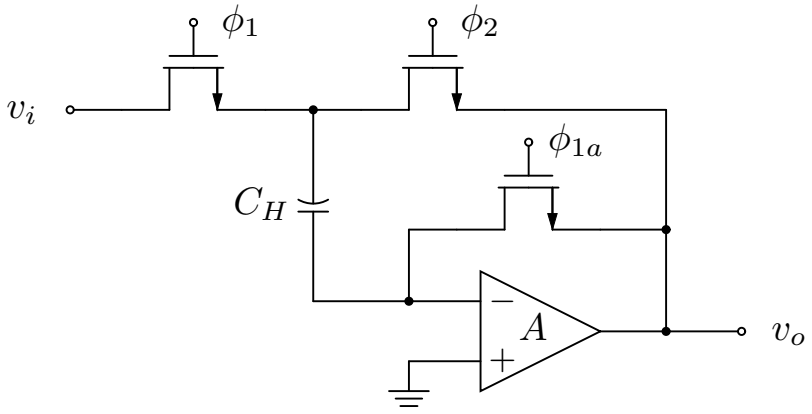




## Switched-Capacitor S/H Circuits

❑ Quite accurate but not necessarily fast → low frequency circuit.

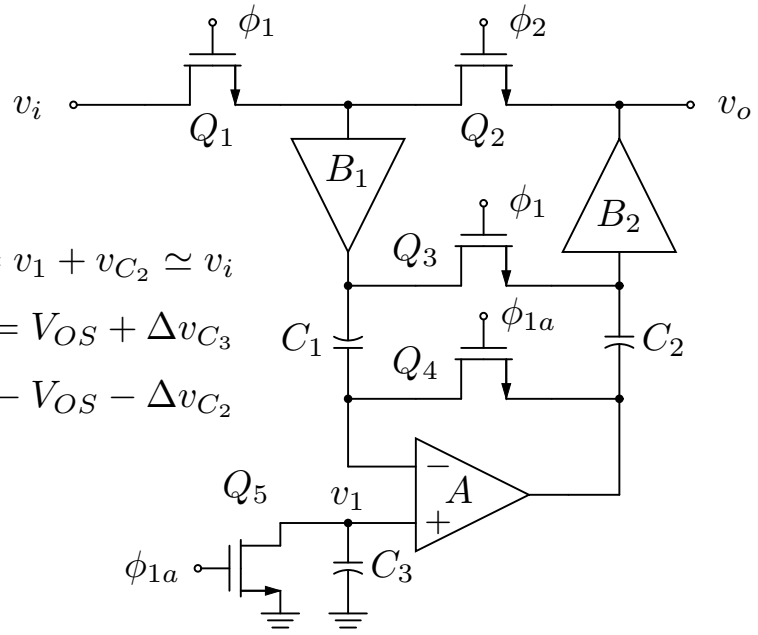
❑ A simple SC S/H: During $\phi_1$, $C_H$ is charged up to $v_i - V_{OS}$ and $v_o = V_{OS}$ (not track). During $\phi_2$, $v_o$ is equal to $v_i - V_{OS} + V_{OS} = v_i$, $\Delta v \neq 0$. Large changes of the opamp output voltage → low speed.






❏ A recycling SC S/H to improve accuracy: charge injections ($Q_4$, $Q_5$: dc offset, cancelled by CMR), ($Q_3$: signal dependent but minimized by Miller effect), ($Q_1$, $Q_2$: no effect due to $B_1$ and $B_2$).

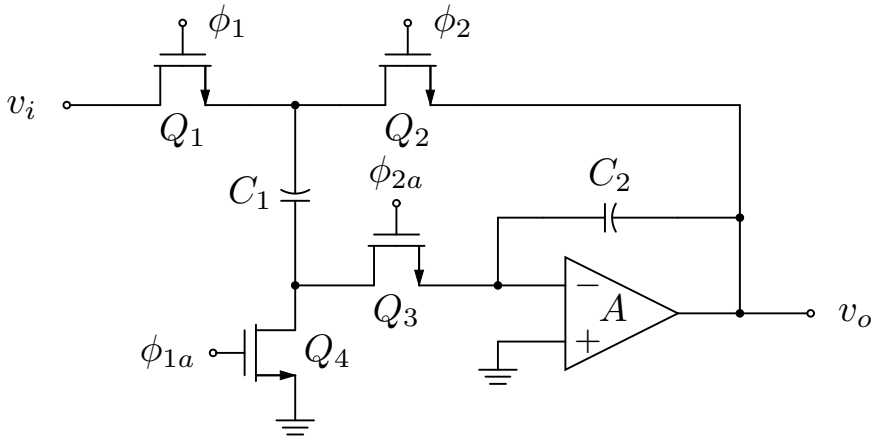
$$v_o = v_1 + v_{C_2} \simeq v_i$$
$$v_1 = V_{OS} + \Delta v_{C_3}$$
$$v_{C_2} = v_i - V_{OS} - \Delta v_{C_2}$$








❏ A switched-capacitor S/H with a low-pass filter: signal conversion from sampled-data domain to continuous-time domain, the charge of $C_1$ is shared with the charge of $C_2$ → LPF, high-Q audio DAC.




❏ Errors: dc offset ($Q_3$, $Q_4$), signal dependent ($Q_2$: reduced by Miller effect), can be minimized by cancellation or differential architecture.

❏ Unlike previous circuits, $V_{OS}$ is not eliminated but $v_o$ is always valid.

❏ Transfer function by discrete-time analysis.

$$v_i(n-1)C_1 + v_o(n-1)C_2 = v_o(n)(C_1+C_2)$$

$$z^{-1}V_i(z)C_1 + z^{-1}V_o(z)C_2 = V_o(z)(C_1+C_2)$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{(C_1+C_2)z - C_2}, \quad z_p = \frac{C_2}{C_1+C_2}$$

❏ Cutoff frequency of the switched-capacitor LPF: $f \ll f_s = 1/T$

$$z = e^{sT} \simeq 1 + sT \quad \text{for } |sT| \ll 1$$

$$H_c(s) = H(z)|_{z=1+sT} = \frac{C_1}{C_1 + s(C_1+C_2)/f_s} = \frac{1}{1+s/\omega_p}$$

$$f_p = \frac{f_s C_1}{2\pi(C_1+C_2)} \simeq \frac{f_s C_1}{2\pi C_2} \quad (C_2 \gg C_1)$$




## Bandgap Voltage Reference Basics

❏ The approaches to realize voltage references in integrated circuits.

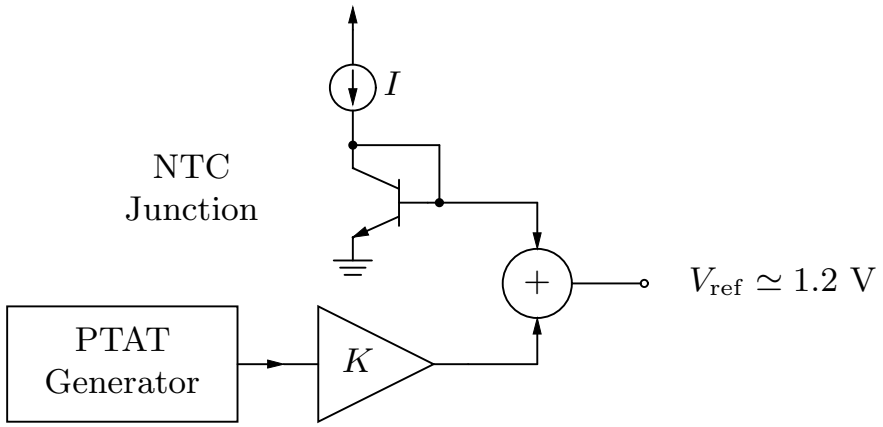
(1) Making use of a Zener diode.
Not popular because breakdown voltage > power supply voltage.

(2) Making use of the difference in $V_t$ between efet and dfet.
Cannot be used in most CMOS circuits because dfet is not available, process sensitivity of reference voltage due to dependence of $V_t$ on doping concentration.

(3) Cancelling NTC of a *pn* junction with PTC (positive temperature coefficient) of a PTAT (proportional to absolute temperature) circuit. Bandgap voltage reference is the most popular for both bipolar and CMOS technologies.


## Bandgap Voltage Reference

❏ A simplified circuit of a bandgap voltage reference.




❏ Bipolar transistor equation.

$$I_C = I_S e^{V_{BE}/V_T} \equiv I_S e^{qV_{BE}/kT} \leftarrow \text{strong dependence on } T$$





❏ Temperature dependence of $V_{BE}$: TC $\simeq -2$ mV/K, $\eta \equiv 4 - n \simeq 2.3$, $n$ = exponential TC of mobility, $T_r$ = reference temperature.

$$V_{BE}(T) = V_G(T) - \left(\frac{T}{T_r}\right) V_G(T_r) + \left(\frac{T}{T_r}\right) V_{BE}(T_r)$$
$$- \eta \left(\frac{kT}{q}\right) \ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right) \ln\left[\frac{I_C(T)}{I_C(T_r)}\right] \leftarrow \begin{array}{c}\text{design} \\ I_C \propto T\end{array}$$

❏ Temperature dependence of silicon bandgap voltage.

$$V_G(T) = a - bT - cT^2, \quad \text{error} < 0.2 \text{ mV}$$

$$\left.\begin{array}{l} a = 1.1785 \text{ V} \\ b = 9.025 \times 10^{-5} \text{ V/K} \\ c = 3.05 \times 10^{-7} \text{ V/K}^2 \end{array}\right\} \quad \text{for } 150 \text{ K} < T < 300 \text{ K}$$



$$\left.\begin{aligned} a &= 1.20595 \text{ V} \\ b &= 2.7325 \times 10^{-4} \text{ V/K} \\ c &= 0 \text{ V/K}^2 \end{aligned}\right\} \quad \text{for } 300 \text{ K} \leq T < 400 \text{ K}$$

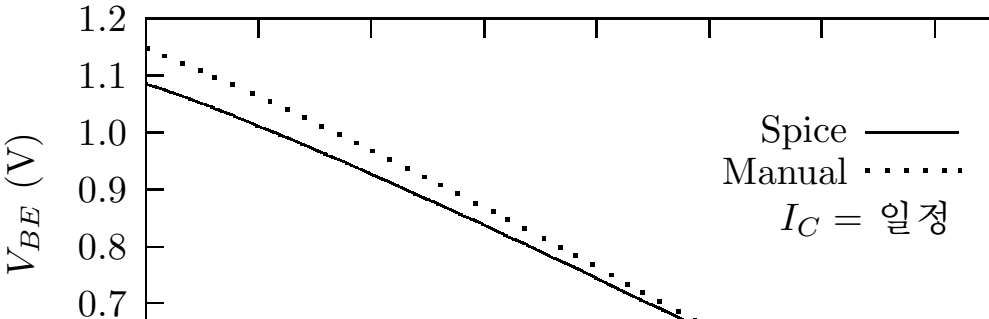
❏ Generation of PTAT voltage: TC $\simeq$ 0.198 mV/K, the difference in two base-emitter junction voltages, quite accurate even if $I_C = f(T)$.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_{C1} I_{S2}}{I_{C2} I_{S1}}\right) \equiv V_T \ln\left(\frac{J_1}{J_2}\right)$$

❏ Bandgap voltage reference $= V_{BE}(T) + K\Delta V_{BE}(T) \simeq 1.235$ V.

$$\begin{aligned} V_{\text{ref}} &= V_G(T) - \left(\frac{T}{T_r}\right) V_G(T_r) + \left(\frac{T}{T_r}\right) V_{BE}(T_r) \\ &- (\eta - 1)\left(\frac{kT}{q}\right) \ln\left(\frac{T}{T_r}\right) + K\left(\frac{kT}{q}\right) \ln\left(\frac{J_1}{J_2}\right) \end{aligned}$$





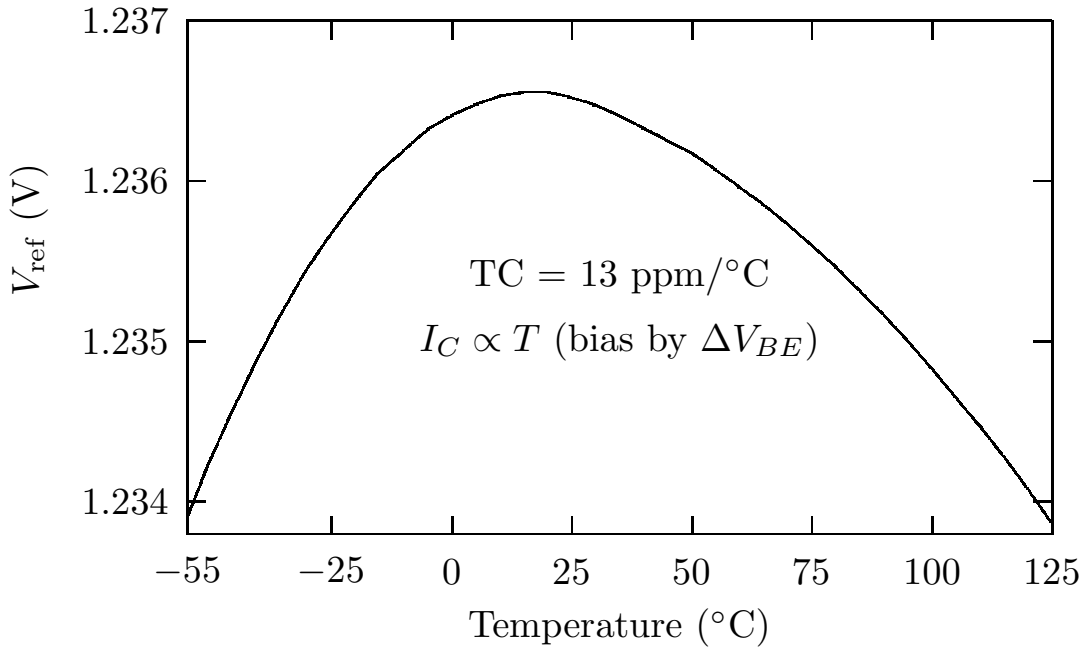


## $V_{BE}$ Plot by Simulation and Calculation






## Ideal Bandgap Reference Voltage



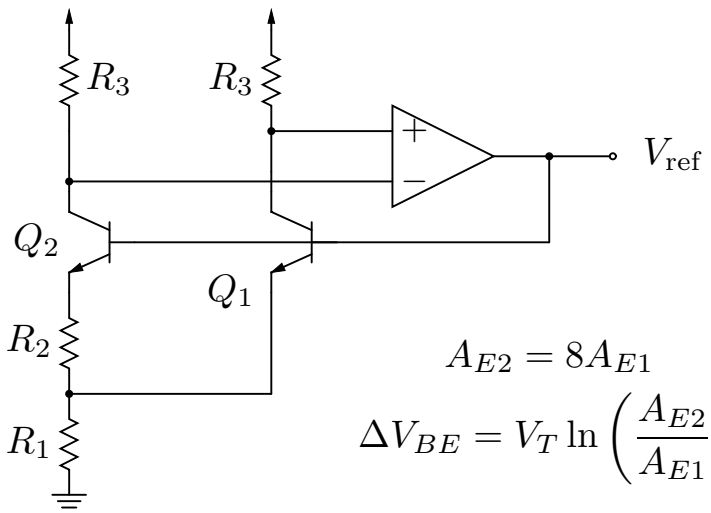





## A Bipolar Bandgap Voltage Reference

❑ Reference voltage: $I_{C1} = I_{C2} \rightarrow I_{E1} = I_{E2} = \Delta V_{BE}/R_2$.

$$V_{\text{ref}} = V_{BE1} + V_{R_1} = V_{BE1} + 2R_1 I_{E2} = V_{BE1} + \frac{2R_1}{R_2}\Delta V_{BE}$$



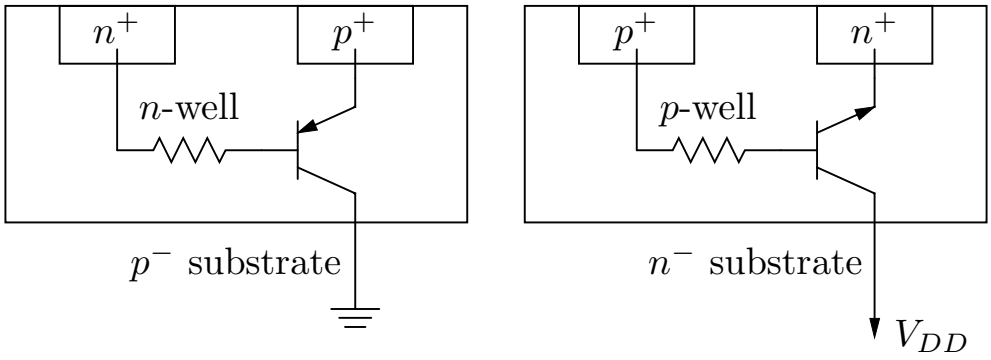

$$A_{E2} = 8A_{E1}$$

$$\Delta V_{BE} = V_T \ln\left(\frac{A_{E2}}{A_{E1}}\right)$$



## Bipolar Transistors in CMOS Processes

❑ *Well transistors*: vertical bipolar transistors use wells as bases and the substrate as collectors, reasonable current gain but large base resistance → $I_C < 0.1$ mA, $n$-well process is the most common CMOS process (*pnp* with grounded collector).



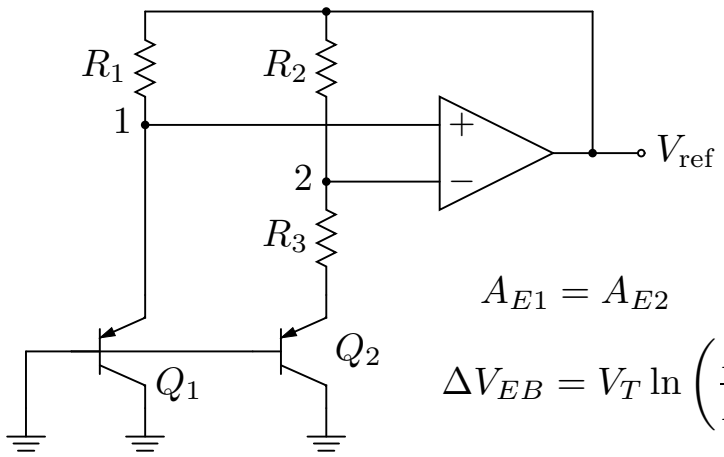





## A CMOS Bandgap Voltage Reference

❑ Bandgap voltage reference in an $n$-well CMOS process.

$$V_{\text{ref}} = V_{EB1} + V_{R_1} = V_{EB1} + V_{R_2} = V_{EB1} + \frac{R_2}{R_3}\Delta V_{EB}$$

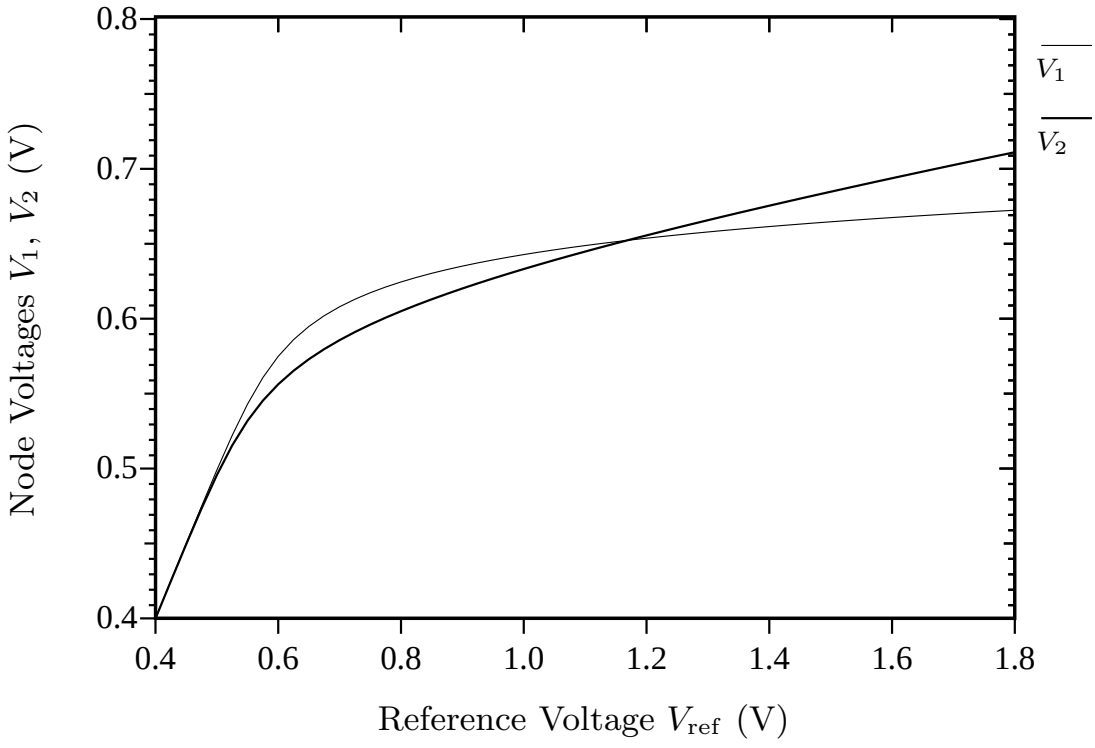



$$A_{E1} = A_{E2}$$

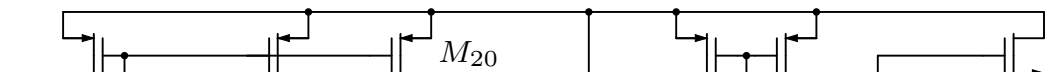
$$\Delta V_{EB} = V_T \ln\left(\frac{R_2}{R_1}\right)$$



❑ Operating points of the bandgap-reference circuit.





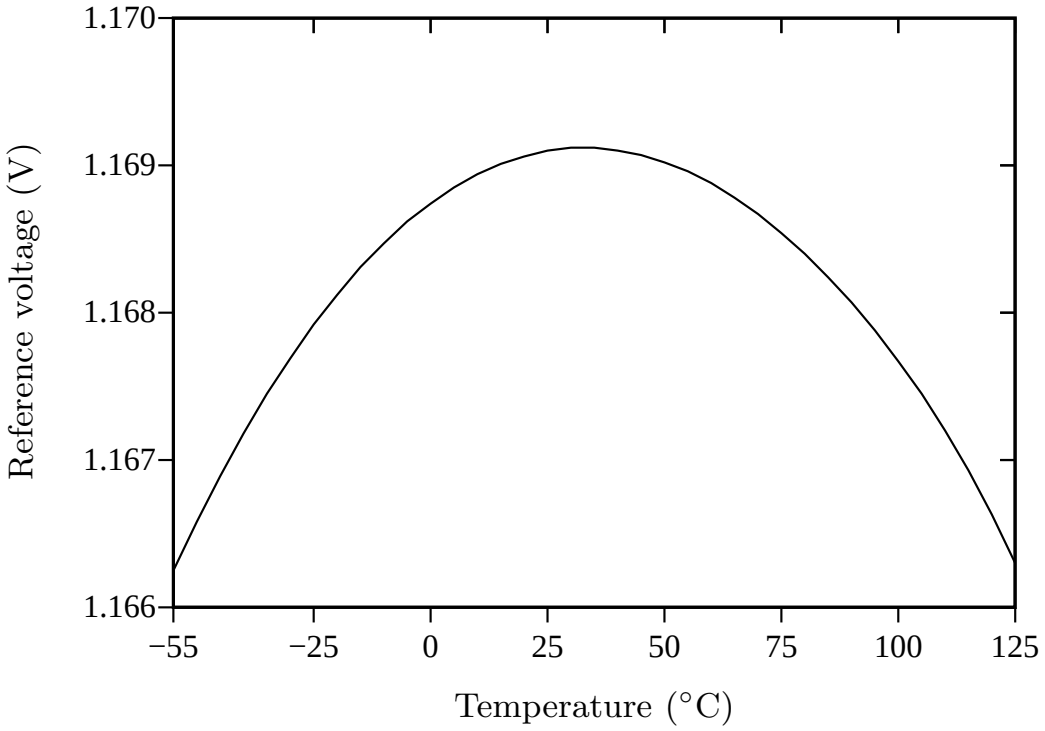


## A CMOS Bandgap Reference Circuit






❏ Temperature variations of the reference voltage $V_{\text{ref}}$: 15 ppm/°C.








## Performances of CMOS Bandgap Reference

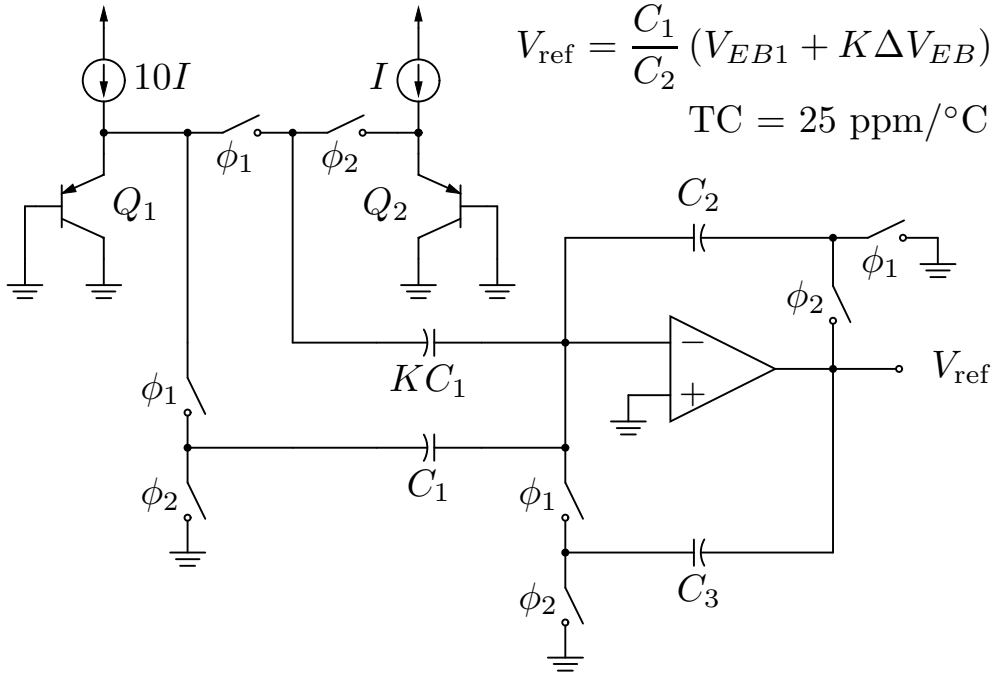
| | |
|---|---|
| Output voltage | 1.168 V |
| Temperature coefficient | 15 ppm/°C |
| Line regulation | 1.29 mV/V |
| Minimum supply voltage | 3.7 V |
| Power-supply rejection ratio | 58 dB |
| Power dissipation @ $V_{DD} = 5$ V | 0.8 mW |

❏ Error sources: temco of well resistors ($\eta = 2.2$), offset voltage $V_{OS}(T)$, second-order effects → SC amplifier, *curvature correction* method.

$$R(T) = R_0 \frac{T^\eta}{T_0^\eta}, \quad \text{TC}_{\text{error}} \simeq 26 \text{ ppm}/^\circ C \text{ for 1 mV offset}$$



## An SC-Based Bandgap Reference




$$V_{\text{ref}} = \frac{C_1}{C_2}\left(V_{EB1} + K\Delta V_{EB}\right)$$

$$\text{TC} = 25 \text{ ppm/°C}$$





## Curvature-Corrected Bandgap Reference

- First-order compensated BGR.

$$\text{TC} \equiv \frac{1}{V_{\text{ref}}}\left(\frac{V_{\max} - V_{\min}}{T_{\max} - T_{\min}}\right) = 20 \sim 60 \text{ ppm/°C}$$

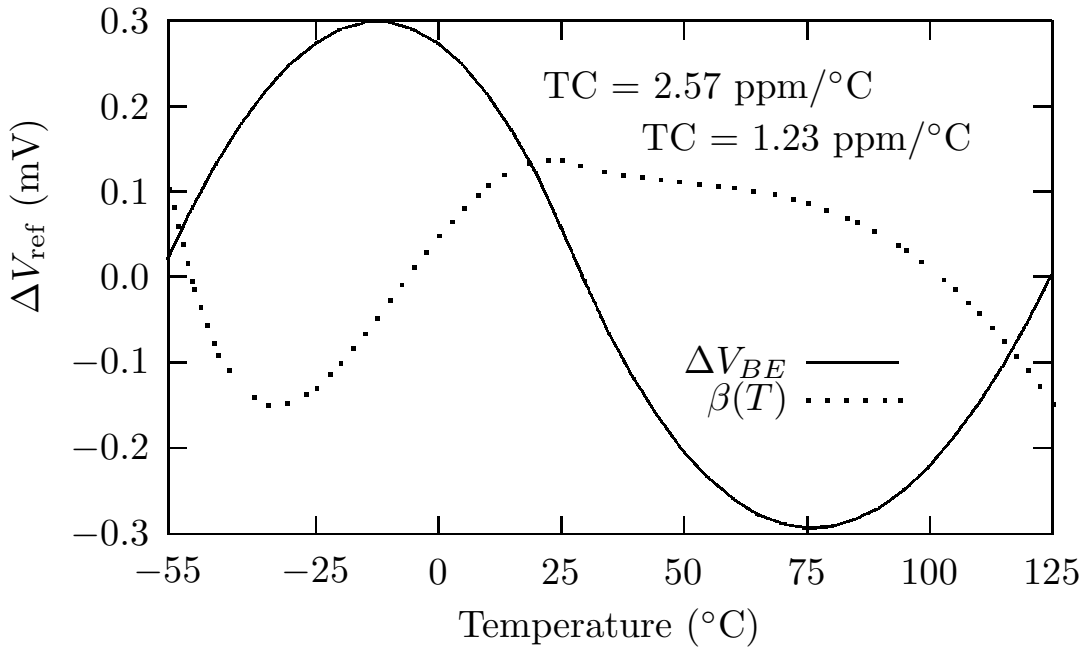
- Curvature-compensation concept: PTAT$^2$, $\beta(T)$, $\Delta V_{BE}$ for transistors biased at a constant and a PTAT current.

$$V_{\text{ref}} = V_{BE} + K_1 V_T + K_2 H(T)$$

- Exponential curvature-compensated BGR: $\Delta E_G$ (bandgap narrowing factor) $\simeq$ 63.9 meV.

$$\beta(T) = \beta_\infty \exp\left(-\frac{\Delta E_G}{kT}\right)$$

## Curvature-Corrected Reference Voltage








## Translinear Gain Cell

- Gilbert gain cell: *pn* junction loads + differential pair, current amplifier, variable gain for continuous-time filters, voltage-controlled amplifiers, analog multipliers (translinear or Gilbert multipliers).
- Voltage difference between emitters: $Q_1$ and $Q_2$ matched, $i_B \approx 0$.

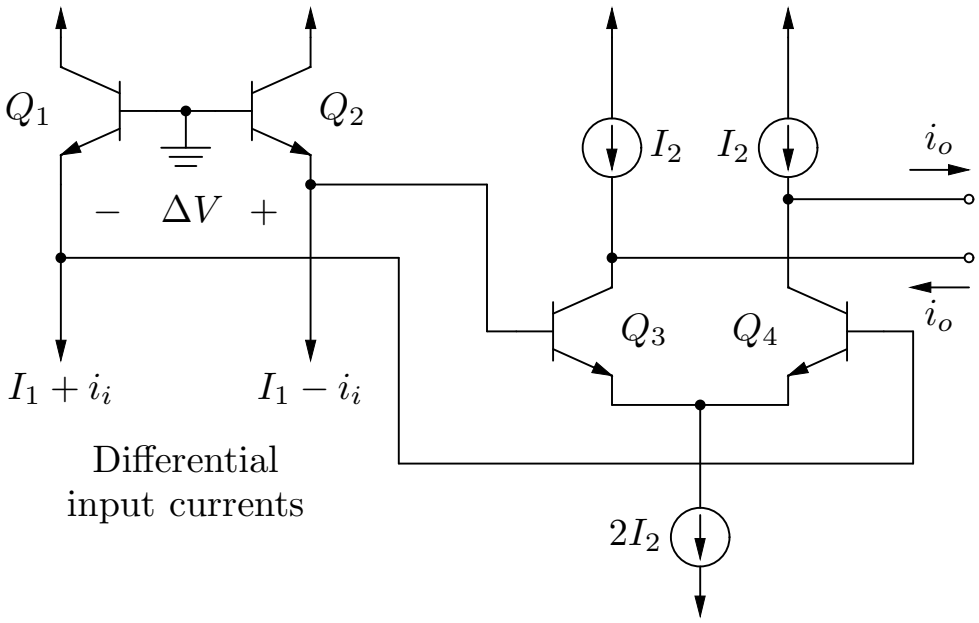
$$\Delta V \equiv v_{E2} - v_{E1} = V_T \ln\left(\frac{I_1 + i_i}{I_1 - i_i}\right) \quad \leftarrow \quad V_{BE} = V_T \ln \frac{I_C}{I_S}$$

- Output current: gain and linearity are not dependent on $\beta$ or $I_S$.

$$i_{C3} = \frac{2\alpha I_2}{1 + e^{-\Delta V/V_T}} = \frac{2\alpha I_2}{1 + \left(\frac{I_1 - i_i}{I_1 + i_i}\right)} = \alpha I_2 + \alpha \frac{I_2}{I_1} i_i \simeq I_2 + \frac{I_2}{I_1} i_i$$

$$i_{C4} \simeq I_2 - \frac{I_2}{I_1} i_i, \quad \therefore i_o = i_{C3} - I_2 = I_2 - i_{C4} \simeq \frac{I_2}{I_1} i_i$$

❏ A translinear gain cell: $i_o \times I_1 = I_2 \times i_i$, analog multiplier: $i_o I_1 = i_1 i_2$.








## Homework

❏ Problems: 8.3, 8.4, 8.6, 8.9, 8.13.

❏ Describe the operation principle of the bandgap reference [1].

## References

[1] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation" *IEEE J. of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, 1999.

[2] W. T. Holman, "New temperature compensation technique for bandgap voltage references", *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 358–388, 1996.

[3] I. Lee, G. Kim, and W. Kim, "Exponential curvature-compensated BiCMOS bandgap references", *IEEE J. of Solid-State Circuits*, vol. 29, no. 11, pp. 1396–1403, 1994.