Basic Opamp Design and Compensation

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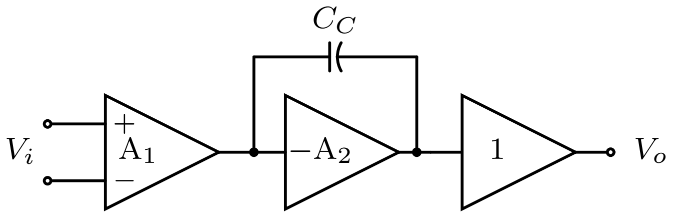
CMOS Opamp Design

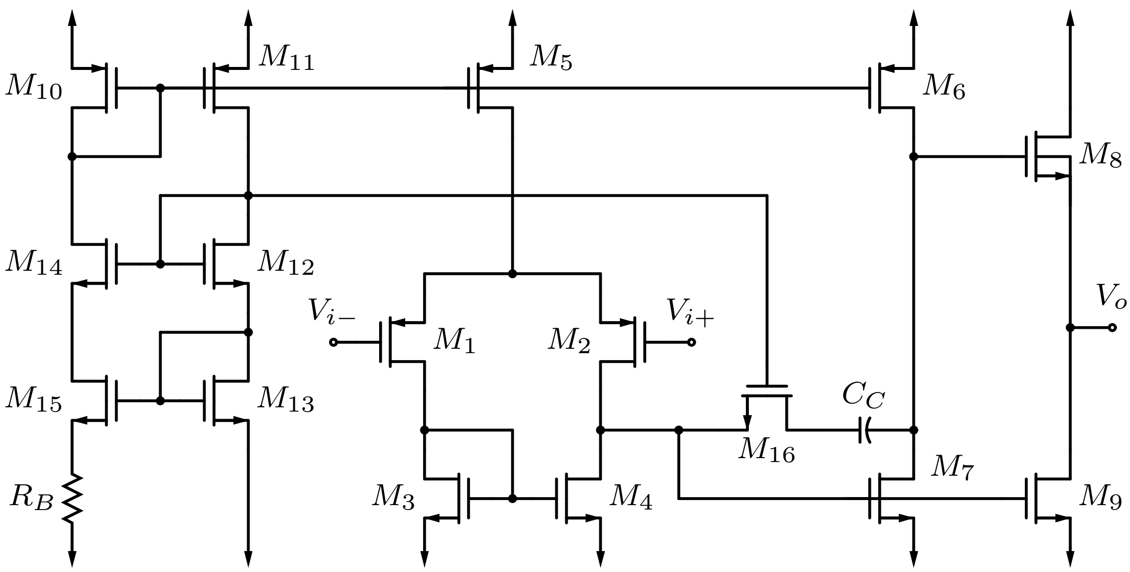
- Fundamental principles of basic opamp design.
- Two-stage CMOS opamp is used to illustrate these principles.
- Compensation techniques for stability when used with feedback.
- Other design techniques: $V_{OS} \to 0$, process-insensitive compensation.
- Biasing circuits of opamps with stability for power-supply voltage, process, and temperature variations.
- Advanced architectures: fully-differential opamps for better noise rejection in high-performance analog and mixed ICs.

Two-Stage CMOS Opamp

- A popular approach for both bipolar and CMOS opamps.
- An excellent example to illustrate design concepts.
- Two-stage = number of gain stages.
- Output buffer is used only when resistive loads need to be driven.
- Differential pair without body effect for better matching.
- C_C = compensation capacitor with Miller effect.
- $L = 1.5 \sim 2$ times the minimum feature size $= 3 \sim 4\lambda$.



- A circuit diagram of a two-stage CMOS operational amplifier.



DC Gain of Opamp

- High DC gain for high accuracy: $A_0 = A_{01}A_{02}A_{03}$
- Gain of the first stage without short-channel effects.

$$-A_{01} = g_{m1}(r_{ds2} \parallel r_{ds4}) \equiv g_{m1}R_{o1}$$

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}, \quad r_{dsi} \approx \alpha \frac{L_i}{I_{Di}}\sqrt{V_{DGi} + V_{ti}}$$

- Gain of the second stage without short-channel effects.

$$-A_{02} = g_{m7}(r_{ds6} \parallel r_{ds7}) \equiv g_{m7}R_{o2}$$

- Gain of the third stage without body effect.

$$A_{03} \simeq \frac{g_{m8}}{g_{m8} + g_{ds8} + g_{ds9} + G_L}$$

Frequency Response of Opamp

- A simplified model: ignore all Cs except C_C, and Q_{16}.
- A capacitive load on the first stage: Miller capacitance.

$$C_M = C_C(1 + A_2) \simeq C_C A_{02}$$

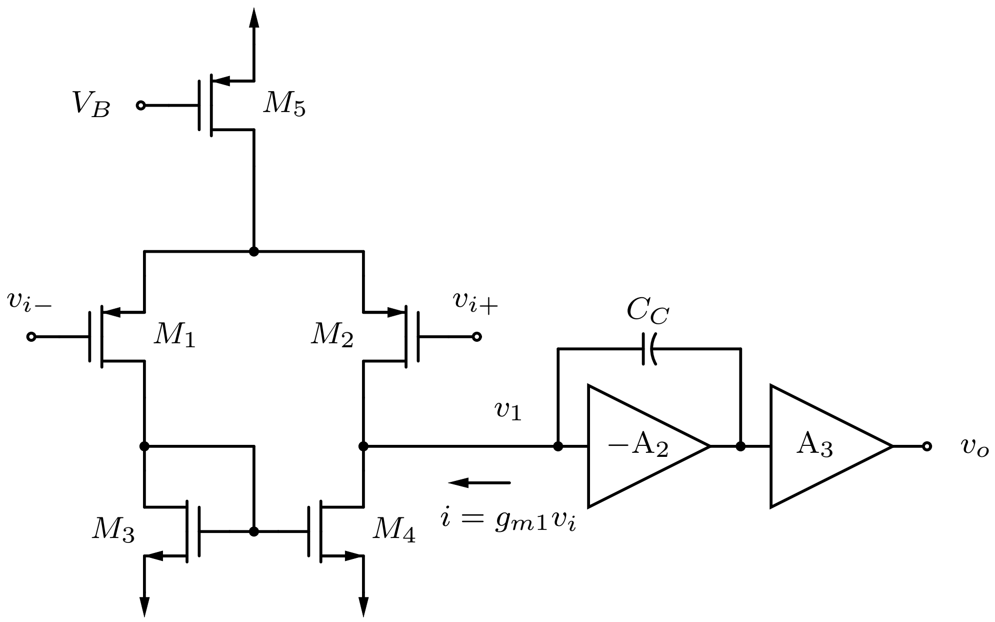
- Frequency response of the first stage: $\omega_{p1} \equiv 1/R_{o1}C_M$.

$$A_1 = \frac{V_1}{V_i} = -g_{m1}\left(r_{ds2} \parallel r_{ds4} \parallel \frac{1}{sC_M}\right) = \frac{-g_{m1}R_{o1}}{1 + sR_{o1}C_M}$$

- Overall frequency response and unity-gain frequency of the opamp.

$$A(s) \equiv \frac{V_o}{V_i} = \frac{A_0}{1 + s/\omega_{p1}} = \frac{g_{m1}R_{o1}A_{02}A_{03}}{1 + sR_{o1}C_M} \simeq \frac{g_{m1}}{sC_C}, \quad \omega_{ta} = \frac{g_{m1}}{C_C}$$

❑ A simplified model used to find the midband frequency response.



Slew Rate of Opamp

❑ Maximum change rate of output for a large input signal.

$$\mathrm{SR} \equiv \left.\frac{dv_o}{dt}\right|_{\max} \simeq \left.\frac{dv_2}{dt}\right|_{\max} = \frac{I_{D5}}{C_C} \quad \left(i \simeq C_C \frac{dv_2}{dt}\right)$$

$$= \frac{2I_{D1}\omega_{ta}}{g_{m1}} = V_{\text{eff1}}\omega_{ta} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}}\,\omega_{ta}$$

❑ For given power dissipation, increase V_{eff1} for large SR → lower g_{m1} $(2I_D/V_{\text{eff1}})$, dc gain, and distortion, higher thermal noise.

❑ Small-signal condition, flicker and thermal noise sources.

$$v_{gs} \ll 2(V_{GS} - V_t), \quad v_g^2(f) = \frac{K}{WLC_{ox}f} + 4kT\left(\frac{2}{3}\right)\frac{1}{g_m}$$

Systematic Offset Voltage

- Design condition for minimum V_{OS}: $I_{D7} = |I_{D6}|$ for $V_{i-} = 0 = V_{i+}$.

$$\frac{I_{D6}}{I_{D5}} = \frac{(W/L)_6}{(W/L)_5} = \frac{I_{D7}}{|I_{D5}|} = \frac{I_{D7}}{2I_{D4}}, \qquad V_{GS4} = V_{DS4} = V_{GS7}$$

$$\therefore \frac{(W/L)_7}{(W/L)_4} = \frac{I_{D7}}{I_{D4}} = 2\frac{(W/L)_6}{(W/L)_5}$$

- Random offset voltage: the voltage drop of the output buffer, any mismatches between the output impedances of p and n MOSTs.

$$V_{OS} \leq 5 \text{ mV}$$

- The input and gain stages of the two-stage opamp.

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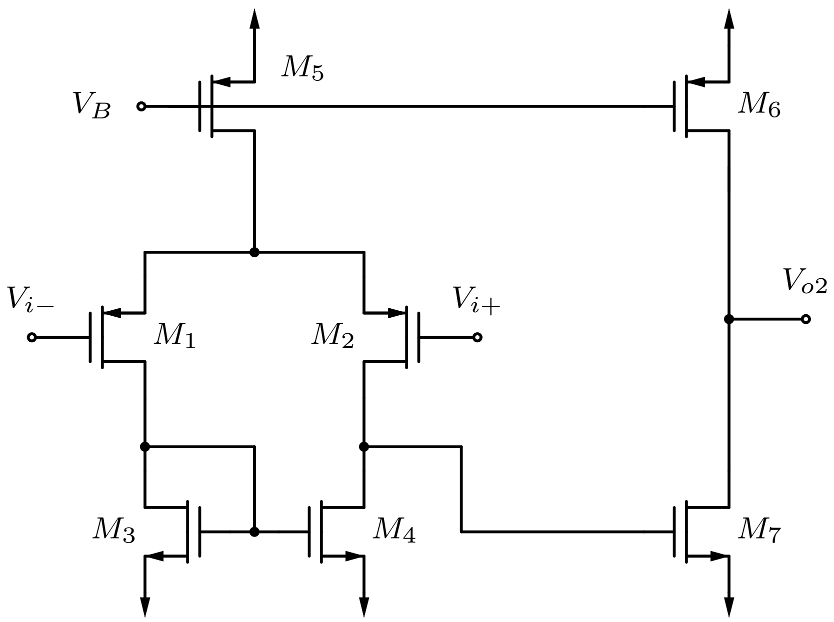


n-Channel or p-Channel Input Stage

- The DC gain: unaffected by the choice since both designs have one stage with nMOSTs and one stage with pMOSTs.
- The structure with pMOST input stage and the second stage with nMOS drive transistor *maximizes* slew rate and g_{m7} for high-frequency operation. ($\tan^{-1}\frac{2}{3} = 33.7°$)

$$\because \ \omega_{ta} < \frac{2}{3}\omega_{p2} \text{ for } 60° \text{ PM}, \quad \omega_{p2} \propto g_{m7}$$

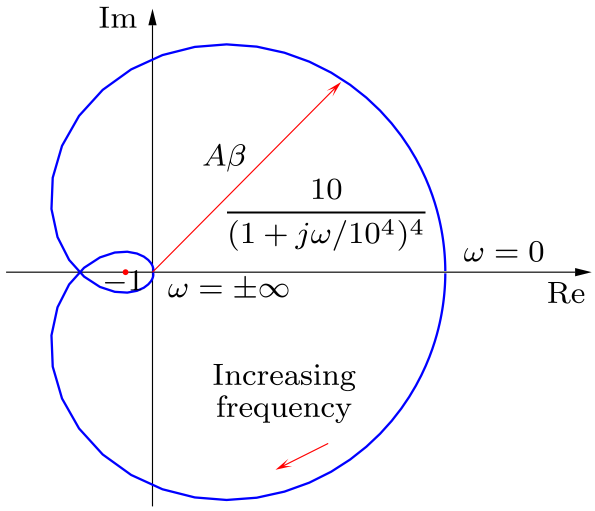
- An nMOST source follower will have less voltage drop V_{GS} for given I_D, less effect of load capacitance C_L on ω_{p2} due to a higher g_m, less degradation of gain for small load resistances.
- pMOSTs have less 1/f noise than nMOSTs but more thermal noise.

Feedback and Opamp Compensation

- Opamps in closed-loop configurations: should be stable at all frequencies as well as over the frequency range of interest.
- How to compensate for good stability and settling characteristics.
- Optimum compensation of opamps: one of the most difficult parts of the opamp design procedure.
- Systematic approach: near-optimum compensation.
- Stable frequency response by biasing to stabilize transconductances for power-supply voltage, process, and temperature variations.

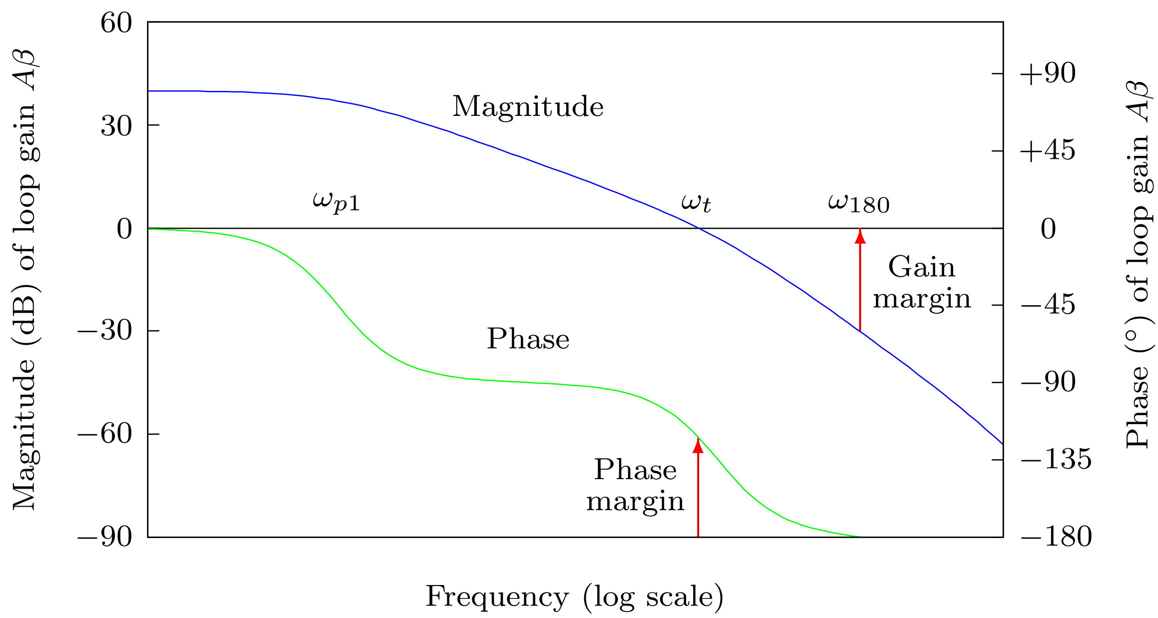
Condition for Stability

- The transient reponse of a stable amplifier must decrease with time.
  $\leftrightarrow$ The poles of A_f must lie in the open left-half s plane ($e^{\sigma_p t} e^{j\omega_p t}$).
- Nyquist criterion: Nyquist plot for loop gain $A\beta$ does not enclose $(-1, 0)$.



Gain and Phase Margins

- Bode plot for the loop gain $A\beta$



First-Order Model of Feedback Amplifier

- Transfer function of a dominant-pole compensated opamp.

$$A(s) = \frac{A_0}{1 + s/\omega_{p1}}$$

- Definition of the unity-gain frequency of an opamp.

$$|A(j\omega_{ta})| \equiv 1 \simeq \frac{A_0}{\omega_{ta}/\omega_{p1}}, \quad \omega_{ta} = A_0\omega_{p1}$$

- Transfer function of feedback amplifiers ($0 \le \beta \le 1$)

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)} = \frac{1/\beta}{1 + 1/\beta A_0 + s/\beta\omega_{ta}} \simeq \frac{1/\beta}{1 + s/\beta\omega_{ta}}$$

- 3-dB frequency: ω_t = unity-gain frequency of loop gain $A\beta$.

$$\omega_{3\text{dB}} \simeq \beta\omega_{ta} \simeq \omega_t$$

Linear Settling Time

- Charge transfer within half a clock period in SC circuits.
- Settling time = nonlinear and linear settling time segments.
- Linear settling time due to finite ω_{ta} for a step input: 1% (0.1%) settling at a time of 4.6τ (7τ), $v_i(t) = V_0 u(t)$, $V_i = V_0/s$

$$V_o = A_f(s)V_i = \frac{V_0/\beta}{s(1 + s/\omega_t)} = \frac{V_0}{\beta}\left(\frac{1}{s} - \frac{1}{s + \omega_t}\right)$$

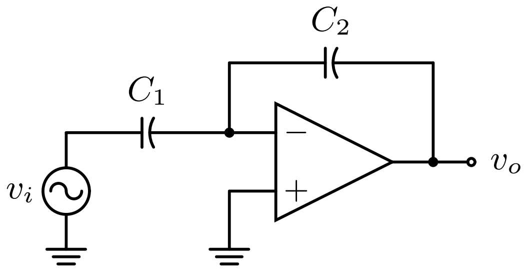
$$v_o(t) = \frac{V_0}{\beta}(1 - e^{-t/\tau})u(t), \quad \tau = \frac{1}{\omega_t} = \frac{1}{\beta\omega_{ta}}$$

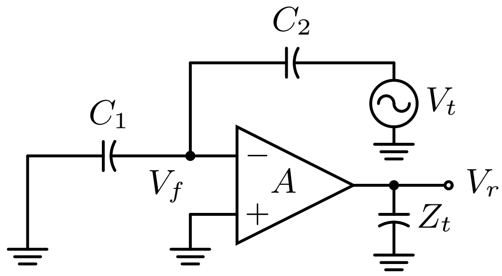
- Nonlinear settling time due to slew-rate limiting.

$$\text{SR} < \left.\frac{dv_o}{dt}\right|_{\max} = \frac{V_0}{\beta\tau} = \omega_{ta}V_0$$

Switched-Capacitor Amplifier

- Amplifier with capacitive feedback during one clock phase: example 5.5





$$C_1 v_i = -C_2 v_o, \quad \frac{v_o}{v_i} = -\frac{C_1}{C_2}, \qquad Z_t = \frac{1}{sC_t}, \quad C_t = \frac{C_1 C_2}{C_1 + C_2}$$

- Two port analysis: unilateral amplifier and feedback network.
- Return ratio analysis: bilateral β, the broken loop is terminated with Z_t

$$\mathcal{R} = A\beta = -\left.\frac{V_r}{V_t}\right|_{Z_t} = -\frac{V_r}{V_f}\frac{V_f}{V_t} = A\left(\frac{C_2}{C_1 + C_2}\right), \quad \omega_{ta} \geq \frac{1}{\tau\beta}$$

Opamp Compensation

- It is important to *accurately* model the transfer function at higher frequencies where the loop gain is unity.
- A model of $A(s)$ by an equivalent pole when all poles and zeros are on the real axis: $1/\omega_{eq} \simeq \sum(1/\omega_{pi}) - \sum(1/\omega_{zi})$, 5% error for $\omega_i > 2\omega_{eq}$

$$A(s) \simeq \frac{A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{eq})} \simeq \frac{\omega_{ta}}{s(1 + s/\omega_{eq})}, \quad \omega \gg \omega_{p1}$$

- The unity-gain frequency ω_t of the loop gain.

$$\mathrm{LG}(s) \equiv \beta A(s) = \frac{\beta\omega_{ta}}{s(1 + s/\omega_{eq})}, \quad \beta\omega_{ta} = \omega_t\sqrt{1 + (\omega_t/\omega_{eq})^2}$$

- The phase margin of the loop gain.

$$\mathrm{PM} = \angle\mathrm{LG}(j\omega_t) - (-180^\circ) = 90^\circ - \tan^{-1}(\omega_t/\omega_{eq})$$

❑ The 2nd-order approximation of $A_f(s)$ near ω_t

$$A_f(s) \simeq \frac{K\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}, \quad \omega_0 \simeq \sqrt{\beta\omega_{ta}\omega_{eq}}, \quad Q \simeq \sqrt{\beta\omega_{ta}/\omega_{eq}}$$

❑ The relationship between PM, ω_t/ω_{eq}, Q factor, overshoot, and $t_s\omega_t$

PM	ω_t/ω_{eq}	Q factor	Overshoot	$t_s\omega_t$
55°	0.700	0.925	13.3%	12.1
60°	0.580	0.817	8.7%	9.5
65°	0.470	0.717	4.7%	7.5
70°	0.360	0.622	1.4%	5.8
75°	0.270	0.527	0.008%	4.5

❑ PM = 80° to 85° for process and temperature variations.

Transfer Function of Two-Stage Opamp

❑ Small signal model of the opamp without output buffer

$$R_1 = r_{ds2} \parallel r_{ds4}, \quad C_1 = C_{db2} + C_{db4} + C_{gs7}$$

$$R_2 = r_{ds6} \parallel r_{ds7}, \quad C_2 = C_{db6} + C_{db7} + C_{L2}$$

❑ Transfer function by nodal analysis: $R_C = 0$, $\omega_{p1} \ll \omega_{p2}$

$$\frac{V_o}{V_i} = \frac{g_{m1}g_{m2}R_1R_2(1 + s/\omega_z)}{1 + as + bs^2}$$

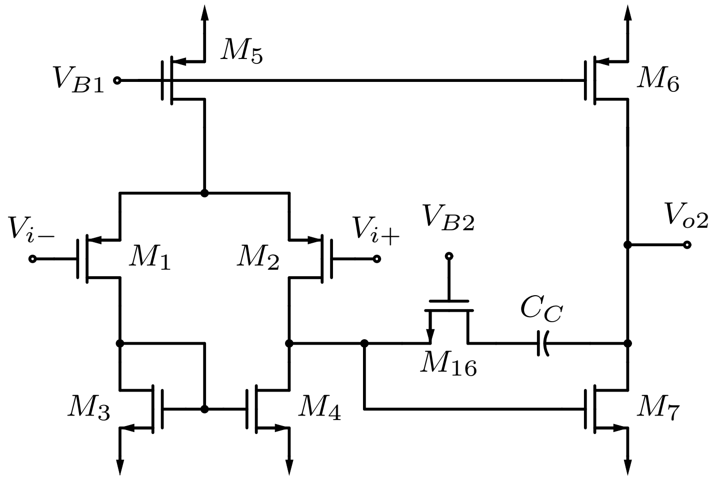
$$a = g_{m7}R_1R_2C_C + R_1(C_1 + C_C) + R_2(C_2 + C_C)$$

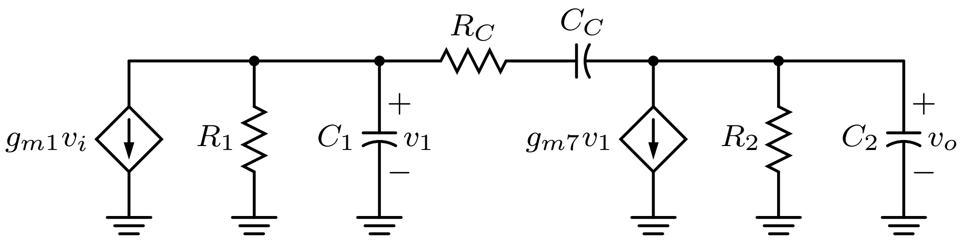
$$b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C), \quad \omega_z = -g_{m7}/C_C$$

$$1 + as + bs^2 = (1 + s/\omega_{p1})(1 + s/\omega_{p2}) \simeq 1 + s/\omega_{p1} + s^2/\omega_{p1}\omega_{p2}$$

$$\omega_{p1} = \frac{1}{a} \simeq \frac{1}{g_{m7}R_1R_2C_C}, \quad \omega_{p2} = \frac{1}{b\omega_{p1}} \simeq \frac{g_{m7}}{C_1 + C_2}$$

- A compensation network and a small signal model of the opamp.





Compensation of Two-Stage Opamp

- Dominant-pole compensation: controls ω_{p1} by C_C.
- Pole-splitting compensation: Miller effect, $R_C = 0$, $\omega_{p1} \ll \omega_{p2}$,
  RHP zero $(1 + s/\omega_z)$ $\rightarrow$ negative phase shift $(\phi_z = \tan^{-1}\frac{\omega}{\omega_z} < 0)$

$$\omega_{p1} \simeq \frac{1}{g_{m7}R_1R_2C_C}, \quad \omega_{p2} \simeq \frac{g_{m7}}{C_1 + C_2}, \quad \omega_z = -\frac{g_{m7}}{C_C}$$

- Transistor Q_{16} as a resistor: $V_{DS16} = 0$ since $I_{D16} = 0$.

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}(W/L)_{16}V_{\mathrm{eff}16}} = \frac{1}{g_{m16}}$$

- Lead compensation: $R_C > 1/g_{m7}$ $\rightarrow$ $\omega_z > 0$, $\phi_z > 0$

$$\frac{V_1}{R_C + 1/(-\omega_z C_C)} = g_{m7}V_1, \quad \omega_z = -\frac{1}{(1/g_{m7} - R_C)C_C}$$

Techniques of Lead Compensation

- Elimination of the RHP zero: $\omega_z = \infty$.

$$\omega_z = -\frac{1}{(1/g_{m7} - R_C)C_C}, \quad R_C = 1/g_{m7}$$

- Movement of the RHP zero into LHP to cancel ω_{p2}: $\omega_z = \omega_{p2}$.

$$R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right)$$

- Movement of the RHP zero to $1.2\omega_t$ in LHP: almost optimum.

$$R_C \gg 1/g_{m7}, \quad \omega_z \simeq \frac{1}{R_C C_C} \simeq 1.2\omega_t, \quad R_C \simeq \frac{1}{1.2\omega_t C_C} = \frac{1}{1.2 g_{m1}}$$

Design Algorithm of Two-Stage Opamp

(1) Choose arbitrarily, $C'_C \simeq 5$ pF ($R_C = 0$).

(2) Find the frequency ω_t where a $-135°$ phase shift exists, and the gain A' at this frequency using Spice $\quad \rightarrow \quad \omega_t = \omega_{eq}$

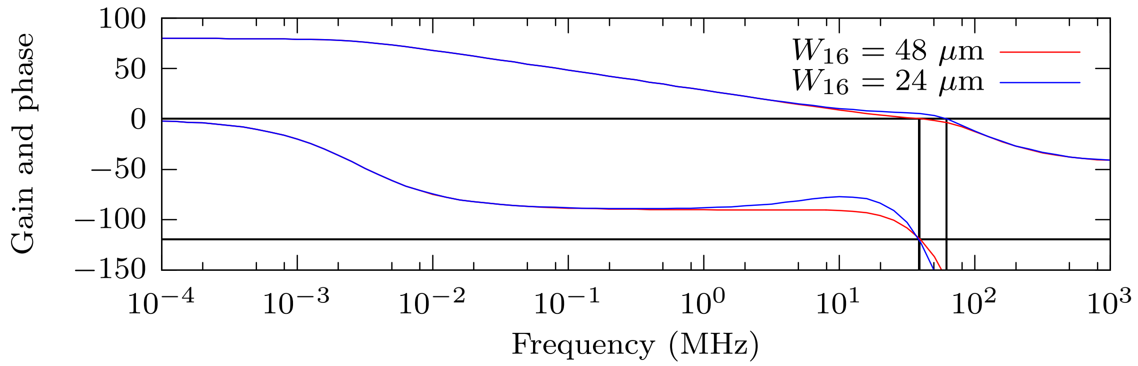
(3) Choose a new C_C so that ω_t becomes the unity-gain frequency of the loop gain: $\mathrm{GB} = g_{m1}/C'_C = A' g_{m1}/C_C \quad \rightarrow \quad C_C = A' C'_C$

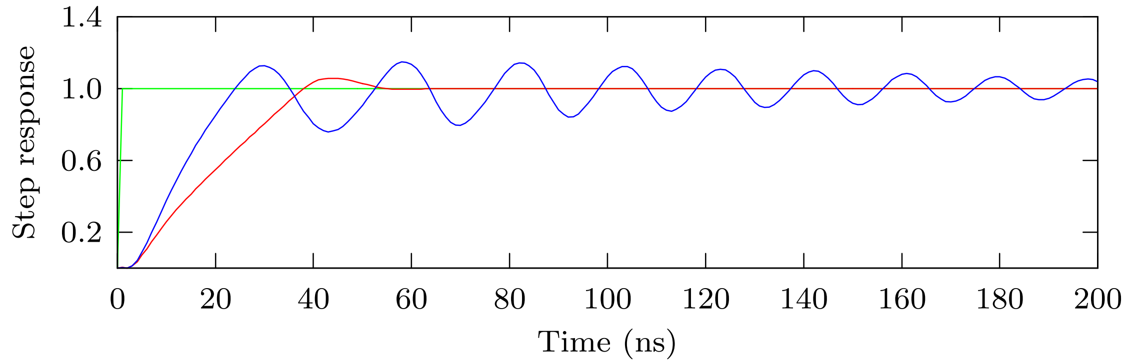
(4) Choose $R_C = 1/1.2\omega_t C_C$ for PM $\simeq 85°$. One should check *frequency doublets* of pole-zero pairs which may cause severe degradation of settling time. $\phi(j\omega_t) = -\angle\frac{\omega_t}{\omega_{p1}} - \angle\frac{\omega_t}{\omega_{eq}} + \angle\frac{\omega_t}{\omega_z} = -90 - 45 + 40 = -95°$

(5) Increase C_C if the phase margin is not adequate.

(6) Replace R_C by a transistor, and tune the device sizes using Spice.

❏ Relationship between phase margin and settling time for channel widths of M_{16}





Compensation Independent of Process and T

❏ Relative positions of pole and zero: $\omega_{ta}/\omega_z \propto (g_{m1}/g_{m7})(g_{m7}R_C - 1)$

$$\omega_{ta} = \frac{g_{m1}}{C_C}, \quad \omega_{p2} \simeq \frac{g_{m7}}{C_1 + C_2}, \quad \omega_z = -\frac{1}{(1/g_{m7} - R_C)C_C}$$

❏ Constant ratios of capacitances by gate oxides.

❏ Constant ratios of transconductances by the same bias network.

$$\frac{I_{D7}}{I_{D13}} = \frac{(W/L)_6}{(W/L)_{11}} \equiv \frac{(W/L)_7}{(W/L)_{13}} \text{ (design rule)} \rightarrow \frac{V_{\text{eff7}}}{V_{\text{eff16}}} \overset{①}{\underset{②}{=}} \frac{V_{\text{eff13}}}{V_{\text{eff12}}}$$

$$(I_D = 0.5\mu_n C_{ox}(W/L)(V_{GS} - V_t)^2 = 0.5 g_m V_{\text{eff}}, \quad I_{D12} \overset{③}{=} I_{D13})$$

$$\therefore g_{m7}R_C = \frac{g_{m7}}{g_{m16}} = \frac{(W/L)_7 V_{\text{eff7}}}{(W/L)_{16} V_{\text{eff16}}} = \frac{(W/L)_7}{(W/L)_{16}}\sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}}$$

Biasing Opamps to Have Stable g_m

- Transistor transconductances are the most important parameters. These must be stabilized over power-supply voltage, process, and T variations.
- Transistor transconductances can be matched to the conductance of a resistor: $(W/L)_{10} = (W/L)_{11}$, $g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}$

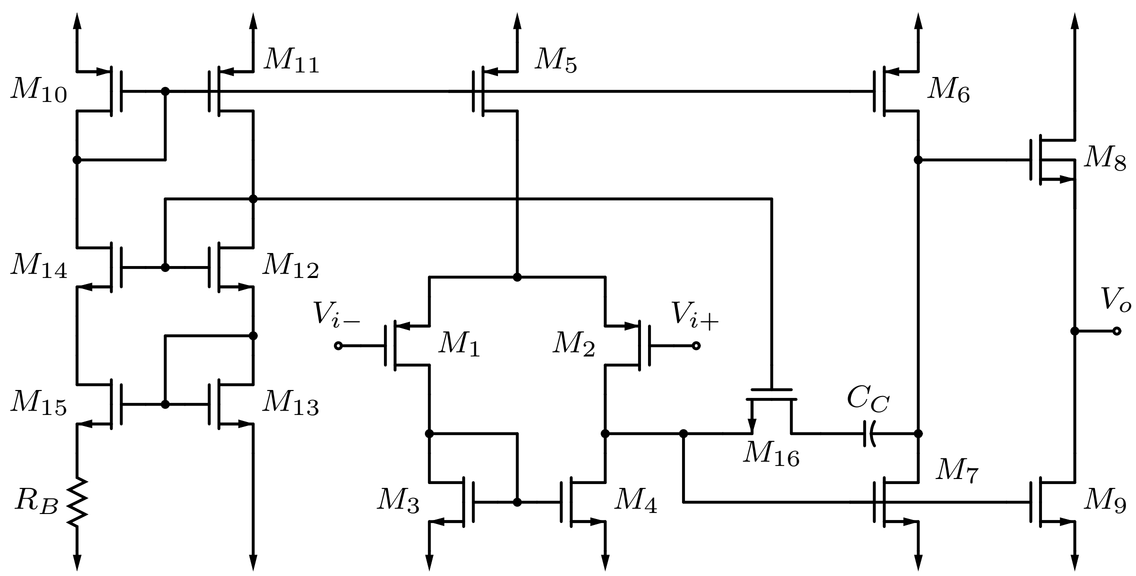
$$V_{GS13} = V_{GS15} + I_{D15}R_B, \quad I_{D13} = I_{D15}$$

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D13}R_B$$

$$\frac{2I_{D13}}{g_{m13}}\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right] = I_{D13}R_B$$

$$g_{m13} = \frac{2\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_B} = \frac{1}{R_B} \quad \text{for} \quad (W/L)_{15} = 4(W/L)_{13}$$

- A two-stage CMOS opamp with a bias circuit that gives very predictable and stable transconductances.



- Stabilized transistor transconductances: $I_{Di} \propto I_{D13}$.

$$\frac{g_{mi}}{g_{m13}} = \frac{\sqrt{2\mu_i (W/L)_i I_{Di}}}{\sqrt{2\mu_n (W/L)_{13} I_{D13}}} = \sqrt{\frac{\mu_i}{\mu_n}\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}} \propto \sqrt{\frac{(W/L)_i}{(W/L)_{13}}}$$

- Second-order effects.
  - Body effect: modify the equation slightly.
  - Transistor output impedance: use wide-swing cascode mirror.
  - Mobility: proportional to $T^{-3/2}$, T increases 300 K to 373 K $\rightarrow V_{\text{eff}}$ increase by 27% for constant $g_{mi} = \mu_i C_{ox} (W/L)_i V_{\text{eff},i}$.

$$\text{Tolerable design value : } 0.2 \text{ V} \leq V_{\text{eff}} \leq 0.25 \text{ V at } 300 \text{ K}$$

  On-chip well or diffusion resistors with PTC: offset this effect.
- A start-up circuit for the bias circuit having positive feedback.

Homework

- Problems: 5.1, 5.2, 5.6, 5.8, 5.10, 5.12, 5.15.
- 그림 5.11의 CMOS 이단 연산 증폭기의 직류 이득, 단위 이득 주파수, 위상 여유, 입력 공통모드 범위, 슬루율, 오프셋 전압, 전력 소모, 출력 전압 범위, 그리고 안정 시간을 `bsim3` 모델을 사용하여 Spice로 구하라. 또한 다른 BSIM1이나 BSIM3 모델 두 가지에 대해서 특성들을 구하고, 세 가지 결과들에 대해 비교 분석하라.

  CMOS 모델은 웹에서 탐색하거나 `www.mosis.org`에서 구할 수 있다. 그리고 회로 입력의 편의를 위해 회로 파일은 `opa2.cir`을 수정 보완하여 사용하라. (PSpice 9.1에서 BSIM3v3.1 모델의 `LEVEL`은 7이다.)
- 그림 5.11의 CMOS 이단 연산 증폭기를 Magic으로 레이아웃하라.