CMOS Comparators

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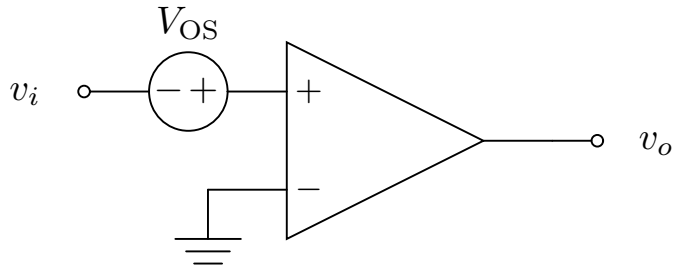
Comparators

- A comparator is used to detect whether a signal is greater or smaller than zero, or to compare the value of one signal to another.
- The second most widely used components after amplifiers.
- Widespread use in A/D converters, data transmission, switching power regulators.
- Using an opamp for a comparator: too slow but a good example to discuss design principles for minimizing V_{OS} and charge injection.
- Other approaches: multistage comparators, positive-feedback track-and-latch comparators, fully differential comparators.

Using An Opamp for A Comparator

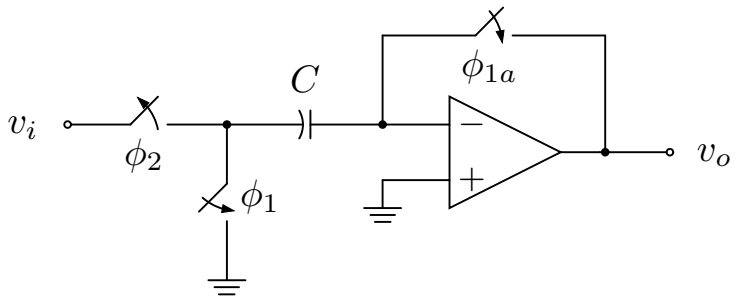
- ❏ Using an open-loop opamp for a comparator.
- ❏ Slow response time due to slewing and settling time.
- ❏ A simple approach.



- ❏ Limited resolution due to V_{OS} of $2 \sim 5$ mV for typical MOS processes.

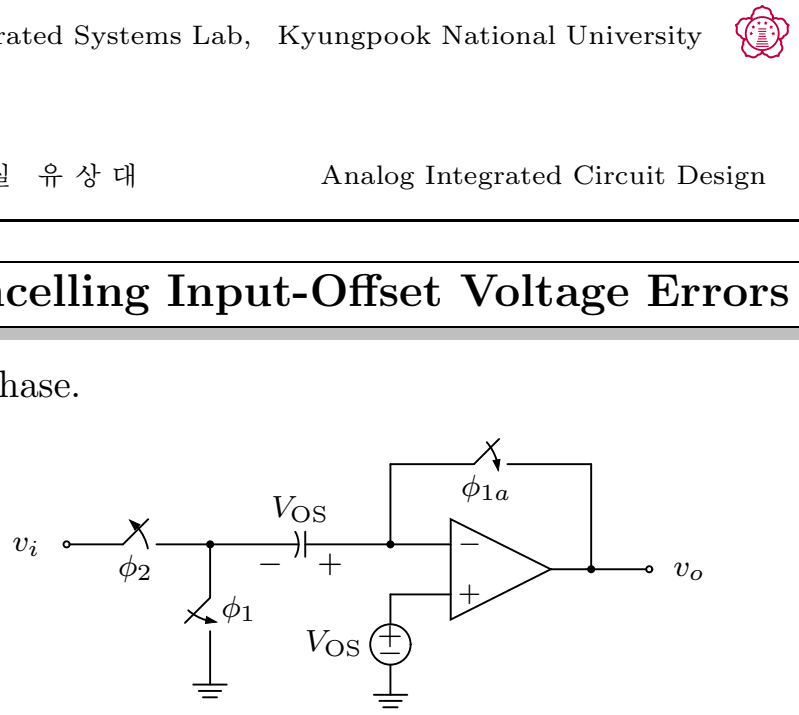
Switched-Capacitor Comparator

- ❏ Operation: reset phase (ϕ_1) + comparison phase (ϕ_2).



- ❏ ϕ_{1a} is a slightly advanced version of ϕ_1 so that charge-injection effects are reduced to the effect due to only the switch ϕ_{1a}.
- ❏ The opamp must be stable for unity-gain feedback during ϕ_{1a}.
- ❏ The bottom plate of integrated capacitors has more significant parasitic capacitance between it and substrate than the top plate.

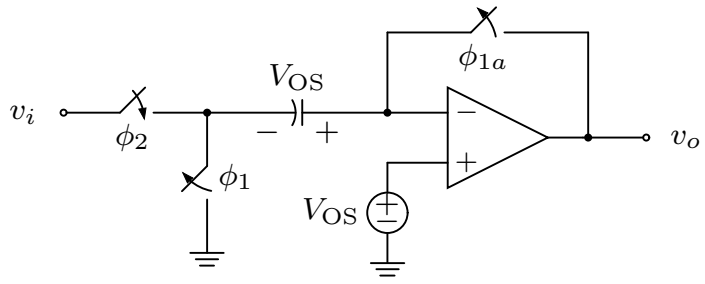
- ❏ Therefore, the bottom plate is always connected to the less sensitive node rather than critical node.
- ❏ Although used in early ADCs, this opproach is not preferable nowadays due to slow operation (500 Hz).
- ❏ A technique for speeding up (50 times) the comparision time is to disconnect the compensation capacitor during the comparision phase.
- ❏ The input capacitor C is never charged or discharged during operation, v_C remains at 0 V. Use a reasonably large C to minimize charge injection and clock-feedthrough effects.
- ❏ If ϕ_1 and ϕ_2 of switches attached to the bottom plate interchanged, the comparision operation would be noninverting. But C must be charged or discharged during reset phase.



Cancelling Input-Offset Voltage Errors

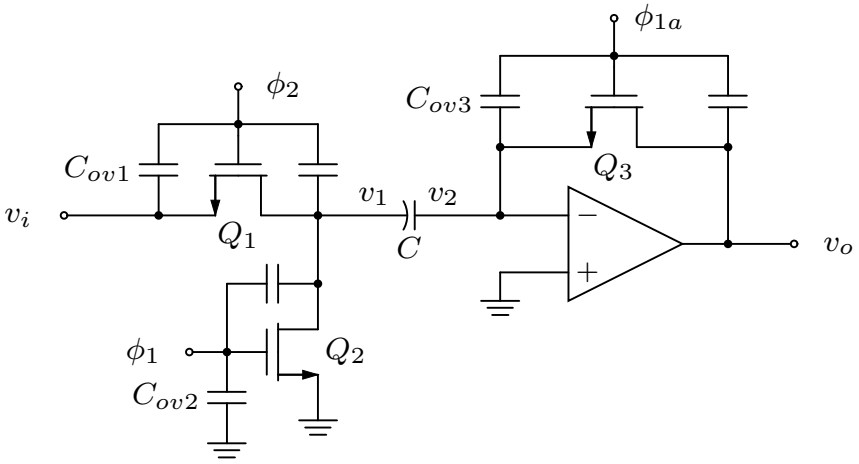
- ❏ The reset phase.

- ❏ The comparision phase.



Charge-Injection Errors

- ❏ Charge injection (clock feedthrough): unwanted charges is injected into the circuit when the transistors turn off.
- ❏ The comparator with switches: channel charge + overlap C.



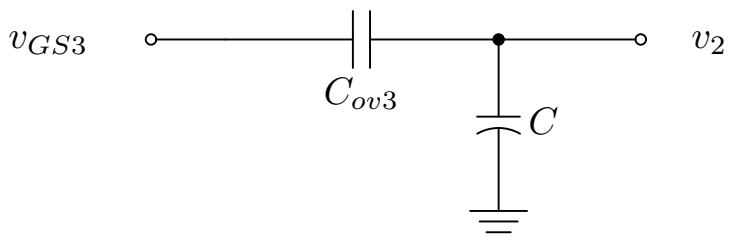
- ❏ Channel charge: $V_{DS} = 0$.

$$Q_{\text{ch}} = WLC_{ox}(V_{GS} - V_t)$$

- ❏ When Q_3 turns off: Δv_{2c} (channel charge) + Δv_{2o} (overlap C).

$$\Delta v_{2c} = \frac{Q_{\text{ch}}/2}{C} = -\frac{C_{ox}W_3L_3V_{\text{eff3}}}{2C} = -\frac{C_{ox}W_3L_3(V_{DD} - V_{tn})}{2C}$$

$$\Delta v_{2o} = -\frac{\Delta v_{GS3}C_{ov3}}{C + C_{ov3}} = -\frac{(V_{DD} - V_{SS})C_{ov3}}{C + C_{ov3}}$$



$$\therefore \text{Resolution} \gg |\Delta v_C| = |\Delta v_{2c} + \Delta v_{2o}| \simeq 13 + 10 = 23 \text{ mV}$$

Making Charge-Injection Signal Independent

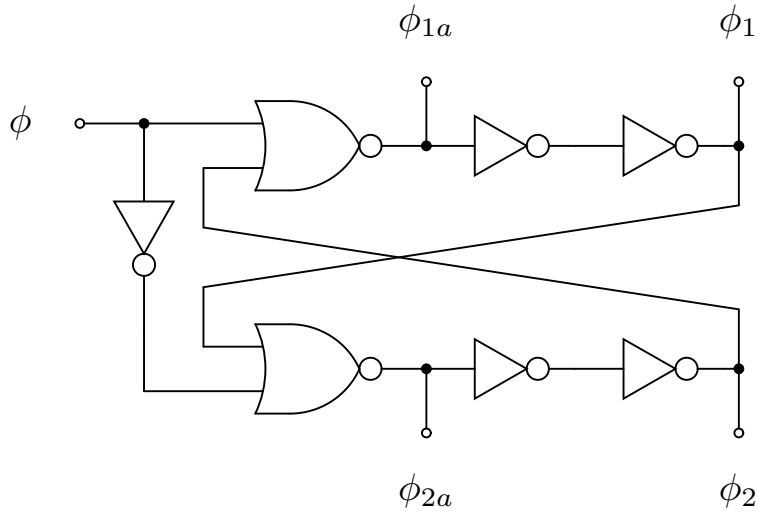
- When Q_2 turns off, its charge injection causes a negative glitch at v_1, but this will *not cause any change in the charge stored in* C since the right side of C is connected to an open node (no current flow).

$$i = C\frac{dv_C}{dt} = 0, \quad \Delta v_C = v_2 - v_1 = 0$$

- Thus, v_2 is unaffected by the charge injection of Q_2. When Q_1 turns on, v_1 will settle to v_i regardless of the charge injection of Q_2. The charge injection of Q_1 has no effect due to similar reason.
- *By turning off* ϕ_{1a} *first, the circuit is affected only by the charge injection of* Q_3. And *the charge injection is signal independent.*

A Clock Generator with Advanced Phases

- Nonoverlapping two-phase clock with phases advanced by two inverter delays.

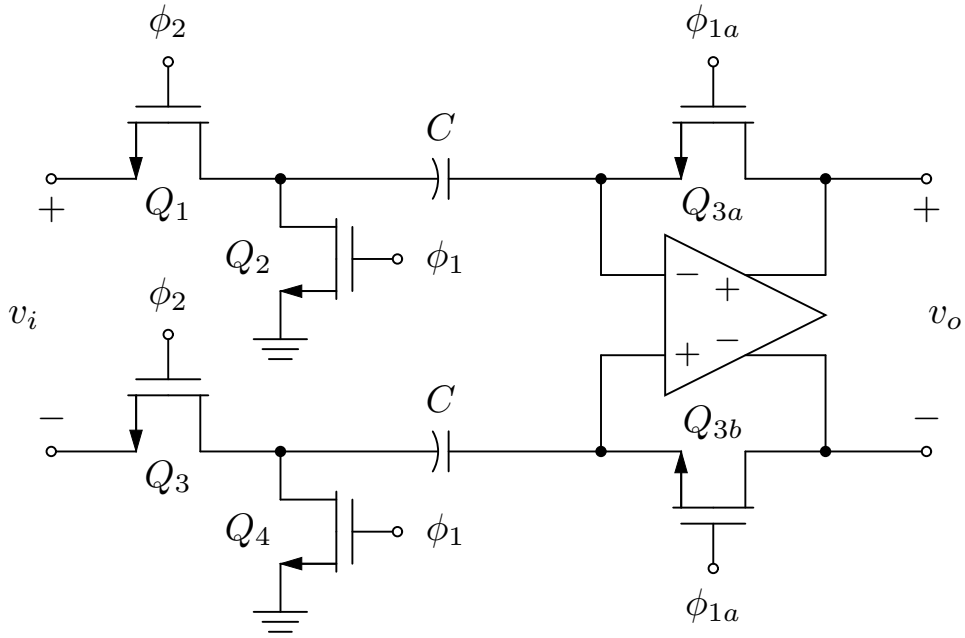


Minimizing Errors Due to Charge Injection

- The simplest way is to use larger capacitors, but this would require a large amount of silicon area: $\Delta v_C \propto 1/C$.
- Integrated capacitors have parasitic capacitances between the bottom plate and the substrate. This bottom plate capacitance might be about 20% of the size of the realized capacitor. This capacitor would have to be driven by the input circuits, which would slow down the circuits.

  A top plate capacitance also exists due primarily to interconnect capacitance, but it is typically on the order of 1 to 5% of the realized capacitance.

- A fully differential switched-capacitor comparator: the charge injection of Q_{3a} matches that of $Q_{3b} \rightarrow \Delta v_C/10$.

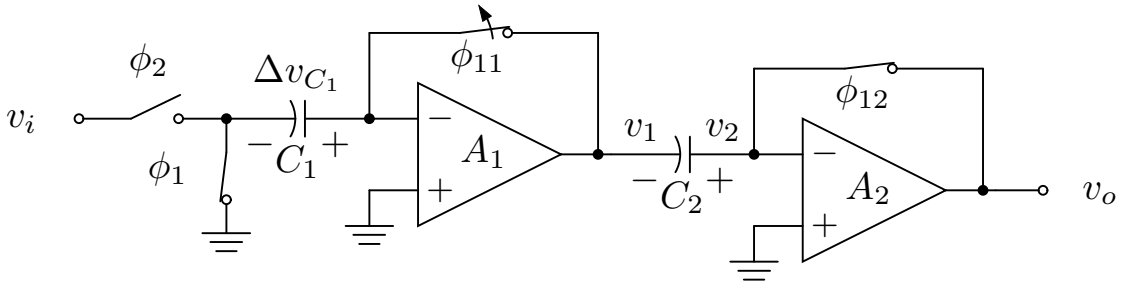


❏ A multistage switched-capacitor comparator: error voltage storing (ϕ_1) + eliminating (ϕ_2), the uncompensated error voltage in the input of the last stage Δv_{C_n}, Δv_{C_1} = charge injection + offset, input equivalent error voltage Δv_i (57 μV), refer to clock waveforms.

$$v_1(\bar{\phi}_{11}) = -A_1(\Delta v_{C_1}) = -v_{C_2}, \quad v_1(\phi_2) = -A_1(v_i + \Delta v_{C_1})$$

$$v_2(\phi_2) = v_1(\phi_2) + v_{C_2} = -A_1(v_i + \Delta v_{C_1}) + A_1\Delta v_{C_1} = -A_1 v_i$$

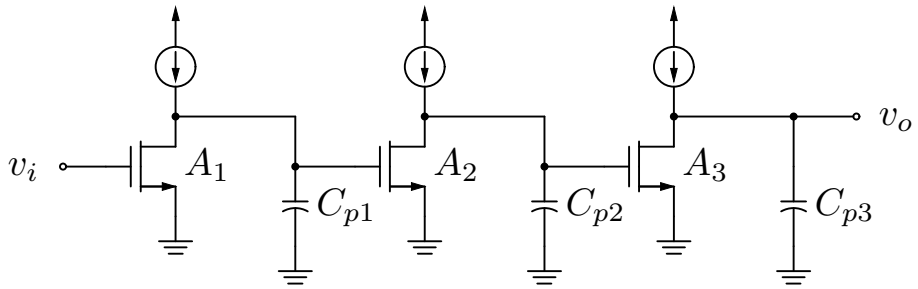
$$v_o = -A_2(v_2 + \Delta v_{C_2}) = A_1A_2\left(v_i - \frac{\Delta v_{C_2}}{A_1}\right) \rightarrow \Delta v_i = \frac{-\Delta v_{C_n}}{A_1A_2\cdots A_{n-1}}$$



Speed of Multistage Comparators

❏ A multistage comparator using a cascade of inverters: very high resolution as combining with fully differential design techniques. Although the multistage comparator has speed limitation due to multiphase clock, it can be reasonably fast and stable because of high-speed individual stages that have only a 90° phase shift.

❏ The parasitic load capacitance of the ith stage: except for the last stage, $C_{pi} \simeq C_{o,i} + C_{gs,i+1} < 2C_{gs,i}$ for large W if $C_{gs} \gg C_o,\ C_r$.



❏ The unity-gain frequency of a single stage i: $C_L = 2C_{gs,i}$.

$$\omega_{ti} \simeq \frac{g_{mi}}{2C_{gs,i}} = \frac{\omega_T}{2}$$

❏ The transfer function of a single stage: dominant-pole approximation.

$$A_i(s) \simeq \frac{A_{0i}}{1 + s/\omega_{pi}}, \quad \omega_{pi} \simeq \frac{\omega_{ti}}{A_{0i}}$$

❏ The overall transfer function of an n-stage comparator.

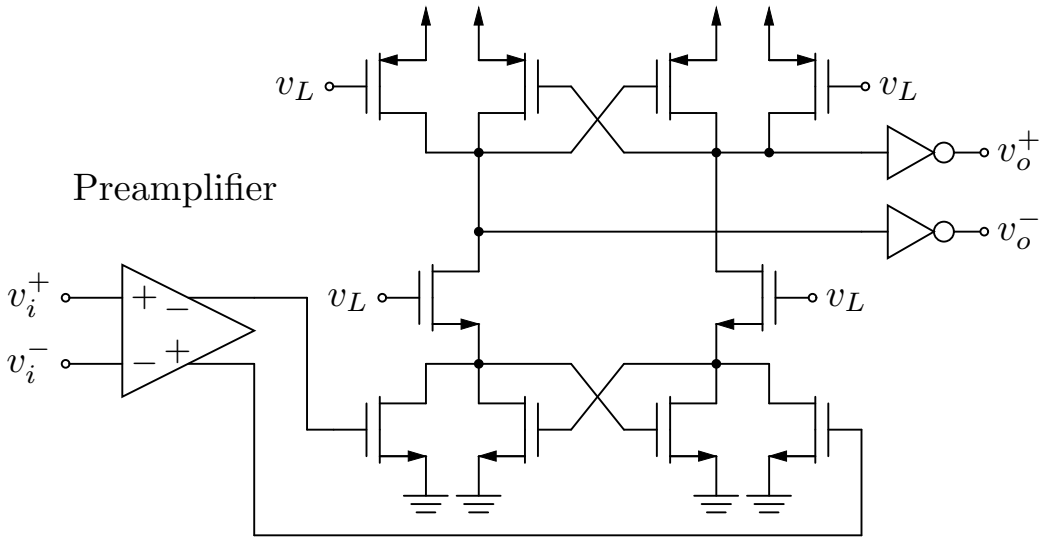
$$A(s) = \prod A_i(s) \simeq \frac{\prod A_{0i}}{1 + s\sum 1/\omega_{pi}} \simeq \frac{A_0^n}{1 + sn/\omega_{pi}}$$

❏ The overall time constant of an n-stage comparator.

$$\tau \simeq \frac{n}{\omega_{pi}} = \frac{2nA_0C_{gs}}{g_m} \simeq \frac{4nA_0L^2}{3\mu_n V_{\text{eff}}} \simeq 4 \text{ ns}$$

Latched Comparators

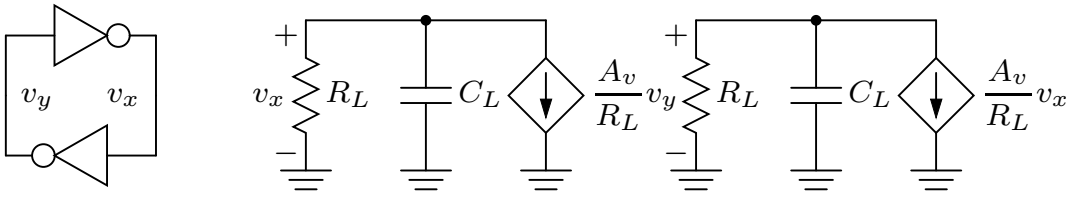
❏ A modern high-speed comparator: preamp + track-and-latch stage.



- Preamplifiers: low gain ($4 \sim 10$) for high speed, used for higher resolution and reduction of kickback effects. *Kickback* denotes the charge transfer either into or out of the inputs when the TAL stage goes from track mode to latch mode. Without a preamplifier, cause very large *glitches* in the input circuit, especially when the input impedances are not perfectly matched → limited accuracy.
- The track-and-latch stage: amplifies the signal further during the track phase, and then amplifies it again during the latch phase by positive feedback → minimizes the total number of gain stages.
- *Hysteresis* might be eliminated by connecting internal nodes to one of power supplies or by connecting differential nodes together (no memory).
- For high resolution, coupling capacitors and reset switches are included to eliminate any V_{OS} and Δv_C errors.

Latch-Mode Time Constant

- Two back-to-back inverters as a simplified model of a TAL stage in the latch phase. The inverters can be modelled as a VCCS driving an RC load for $v_x \simeq v_y$.



- Node equations by KCL: $\tau_L = R_L C_L$, $\Delta v \equiv v_x - v_y$.

$$\tau_L \frac{dv_x}{dt} + v_x + A_v v_y = 0, \quad \tau_L \frac{dv_y}{dt} + v_y + A_v v_x = 0$$

$$\left(\frac{\tau_L}{A_v - 1}\right)\left(\frac{d\Delta v}{dt}\right) = \Delta v$$

❏ Voltage difference between the output voltages of inverters.

$$\Delta v = \Delta v_0 e^{(A_v - 1)t/\tau_L} \equiv \Delta v_0 e^{t/\tau}$$

❏ Latch-mode time constant: $C_L \simeq k_1 WLC_{ox}$, $G_m \simeq k_2 g_m$.

$$\tau = \frac{\tau_L}{A_v - 1} \simeq \frac{R_L C_L}{A_v} = \frac{C_L}{G_m} = \frac{k_1}{k_2}\frac{L^2}{\mu_n V_{\text{eff}}} = (2 \sim 4)\frac{L^2}{\mu_n V_{\text{eff}}}$$

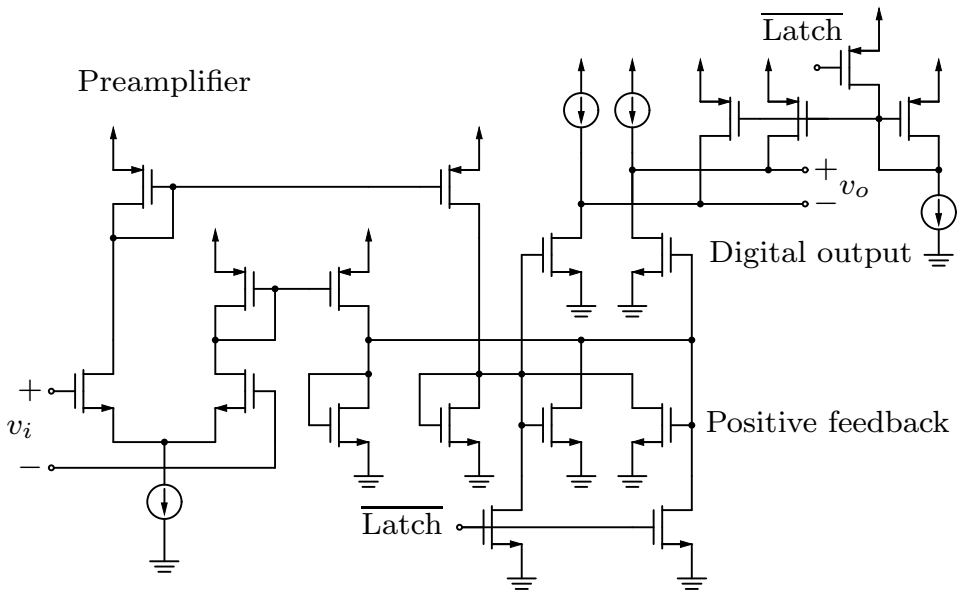
❏ The latch time for a voltage difference $\Delta v \rightarrow \Delta v_L$ (valid logic voltage) $\rightarrow$ the speed would be limited by preamplifiers and TAL during track phase.

$$t_{\text{latch}} = \tau \ln\left(\frac{\Delta v_L}{\Delta v_0}\right) \simeq 0.5 \text{ ns} \rightarrow 1 \text{ GHz}$$

❏ If Δv_0 is small, the rise time can be larger than the allowed time for the latch phase $\rightarrow$ undetermined logic value for succeeding circuitry. This is called *metastability*. Even when Δv_0 is large enough, circuit noise can cause Δv_0 to become small enough to cause metastability.

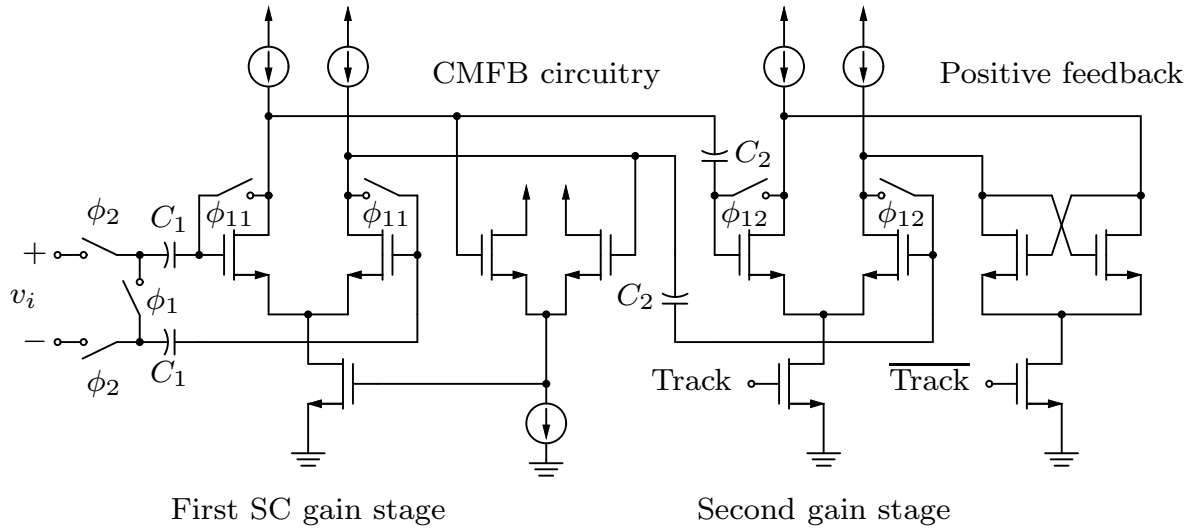
A Two-Stage Comparator with Digital Output

❏ Low-impedance nodes and diode-connected loads for high speed, precharging nodes to eliminate hysteresis, fully differential comparator.



A Two-Stage Comparator with Capacitive Coupling

❏ Capacitive coupling to eliminate V_{OS} and charge-injection errors: resolution $\Delta v < 0.1$ mV at a 2-MHz clock frequency for 5-μm technology.



Homework

❏ Problems: 7.1, 7.6, 7.7, 7.8, 7.11.

❏ Describe the operation principle and the important properties of the comparator used in [1].

References

[1] Y. T. Wang and B. Razavi, "An 8-Bit 150-MHz CMOS A/D Converter", *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, pp. 308–317, 2000.

[2] A. Worapisher, J. B. Hughes, and C. Toumazou, "Speed and accuracy enhancement techniques for high-performance switched-current comparators", *IEEE J. of Solid-State Circuits*, vol. 36, no. 4, pp. 687–690, 2001.