Oversampling Converters

劉 尙 大 敎授

전 자 공 학 부

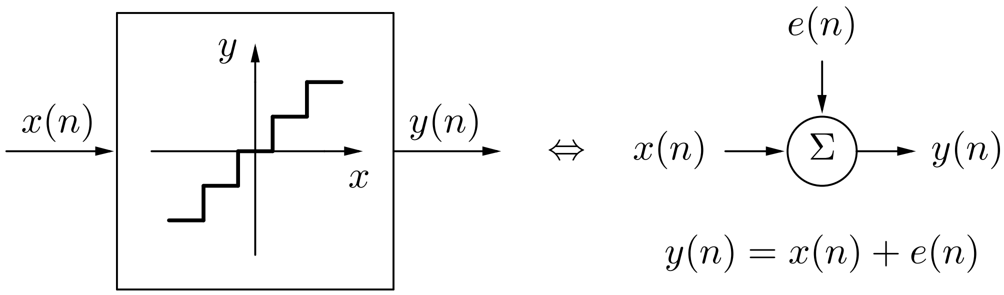
Kyungpook National University

Oversampling Converters

- Recently popular for high-resolution medium-to-low-speed applications such as high-quality digital audio.
- *Reduced requirements* on the analog circuitry at the expense of more complicated high-speed digital circuitry.
- Only a first-order antialiasing filter is required for A/D converters.
- A S/H is usually not required at the input of an oversampling A/D converter with a SC modulator.
- Extra resolution by sampling much *faster* than the Nyquist rate.
- Extra resolution in lower oversampling rates by spectrally *shaping* the quantization noise ($\Delta\Sigma$ modulation).

Oversampling without Noise Shaping

- A linear model of quantizers.



$$y(n) = x(n) + e(n)$$

- Quantization noise (error) modeling: *white noise approximation* for very active $x(n) \rightarrow$ a random number uniformly distributed between $\pm V_{\mathrm{LSB}}/2$ ($V_{\mathrm{LSB}} \equiv \Delta$), normalized noise power of $V_{\mathrm{LSB}}^2/12 \equiv \int S_n^2 df$, root spectral density $S_n(f) = V_{\mathrm{LSB}}/\sqrt{12 f_s}$ for $|f| \leq f_s/2$ (two-sided definition of noise power) or $0 \leq f \leq f_s$ (one-sided definition).

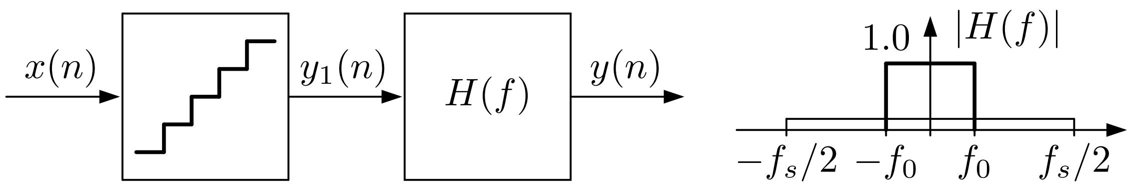
Oversampling Advantage

- Oversampling ratio: Nyquist rate = $2f_0$, OSR $\equiv f_s/2f_0$.
- Maximum SNR: ratio of maximum sinusoidal power to quantization noise, signal amplitude = $V_{\mathrm{ref}}/2 = \Delta 2^N/2$.

$$P_s = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}, \quad P_n = \int_{-f_s/2}^{f_s/2} S_n^2(f)|H(f)|^2 df = \frac{1}{\mathrm{OSR}} \frac{\Delta^2}{12}$$

$$\mathrm{SNR}_{\mathrm{max}} = 10\log(P_s/P_n) = 6.02\mathrm{N} + 1.76 + 10\log(\mathrm{OSR})$$

$$\therefore \text{SNR improvement} \simeq 3 \text{ dB/octave} \simeq 0.5 \text{ bit/octave}$$



- If eight samples of a signal are averaged, this low-pass filtering results in the OSR being approximately equal to 8.

$$\therefore \text{SNR improvement} = 10\log(8) = 9 \text{ dB}$$

- For a 1-bit A/D converter with 6-dB SNR, what is f_s required using oversampling to obtain a 96-dB SNR if $f_0 = 25$ kHz?

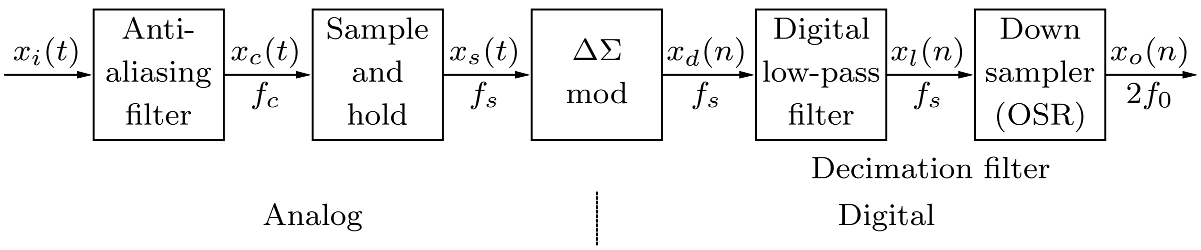
$$f_s \simeq 2^{(96-6)/3} \times 2f_0 \simeq 54,000 \text{ GHz } (33,187 \text{ GHz})$$

$\therefore$ *Noise shaping* is needed to improve the SNR more faster.

- Oversampling does not improve linearity. If a 16-bit ADC is designed using a 12-bit converter with oversampling, the 12-bit converter must have an integral nonlinearity error better than 16-bit accuracy ($1/2^{16}$ = 0.0015 %). 1-bit D/A converters with only two values which define a straight line have *inherent linearity.* → realization of 16 to 20-bit linear ADCs using noise shaping without trimming

Oversampling with Noise Shaping

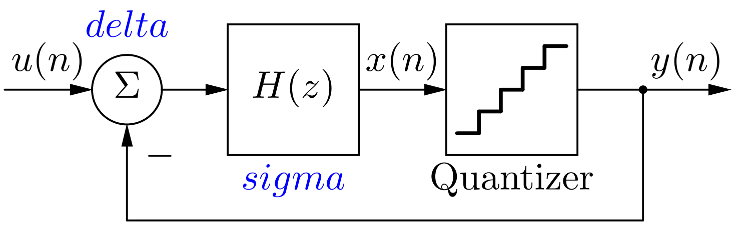
- The system architecture of a ΔΣ oversampling A/D converter.
- Antialiasing filter: $f_c \leq f_s/2$, a simple RC LPF for large OSR.
- *Delta-sigma modulator*: converts the analog signal into a noise-shaped low-resolution digital signal. For a SC ΔΣ modulator, a separate S/H is not required.
- *Decimator*: converts the oversampled low-resolution digital signal into a high-resolution digital signal at a lower sampling rate.

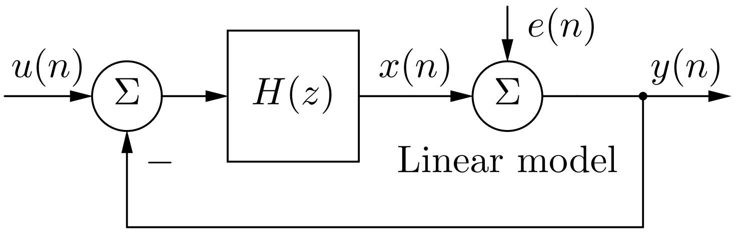


Noise-Shaped Delta-Sigma Modulator

- Transfer function of a delta-sigma modulator: For noise shaping, the magnitude of $H(z)$ is *large* from 0 to f_0, but that of $N(z)$ is *small*.

$$Y(z) = \frac{H(z)U(z)}{1+H(z)} + \frac{E(z)}{1+H(z)} \equiv S(z)U(z) + N(z)E(z)$$





First-Order Noise Shaping

- The z-transform and the Laplace transform: two-sided definitions ($z \equiv e^{sT}$)

$$X(z) \equiv \sum_{n=-\infty}^{\infty} x(n)z^{-n}, \quad X(s) \equiv \int_{-\infty}^{\infty} x(t)e^{-st}dt$$

- Unit delay $H(z) = z^{-1}$: $k = 1$.

$$\sum_{n=-\infty}^{\infty} x(n-k)z^{-n} = \sum_{n=-\infty}^{\infty} x(m)z^{-m}z^{-k} = X(z)z^{-k}$$

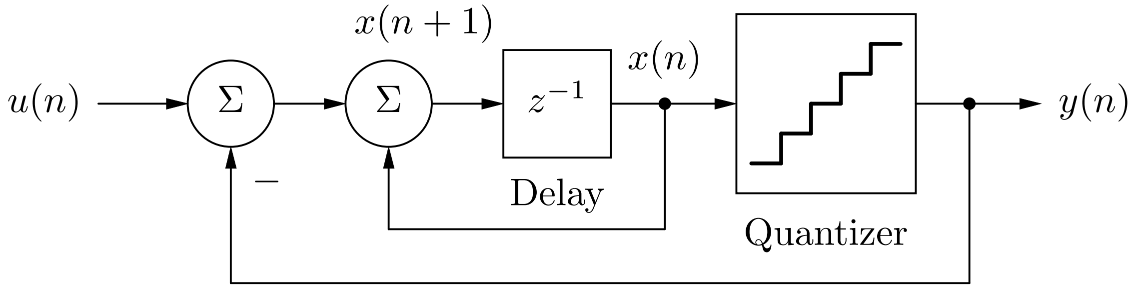
- The noise transfer function $N(z)$ should have a zero (a pole of $H(z)$) at dc ($z = e^{sT} = 1$) → high-pass filtering for noise.
- *A discrete-time integrator*: low-pass filter, accumulator.

$$H(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}} \quad \leftrightarrow \quad y(n) = y(n-1) + x(n-1)$$

Time Domain View

- Since the integrator has infinite dc gain, the average value of $u(n) - y(n)$ *equals zero*. $y(n) = u(n-1) + e(n) - e(n-1)$
- Example: $x(0) = 0.1$, ± 1.0 quantizer with threshold at zero.

n	$u(n)$	$x(n)$	$y(n)$	$e(n)$	$x(n+1)$
0	1/3	0.1	1.0	0.9	−0.5667
1	1/3	−0.5667	−1.0	−0.4333	0.7667
2	1/3	0.7667	1.0	0.2333	0.1



Frequency Domain View

- Signal and noise transfer functions: *delay*, *differentiator* (HPF).

$$S(z) = \frac{H(z)}{1+H(z)} = z^{-1}, \quad N(z) = \frac{1}{1+H(z)} = 1 - z^{-1}$$

- Frequency response for noise: $z = e^{j\omega T} = e^{j2\pi f/f_s}$.

$$N(f) = 1 - e^{-j2\pi f/f_s} = 2je^{-j\pi f/f_s} \sin\left(\frac{\pi f}{f_s}\right)$$

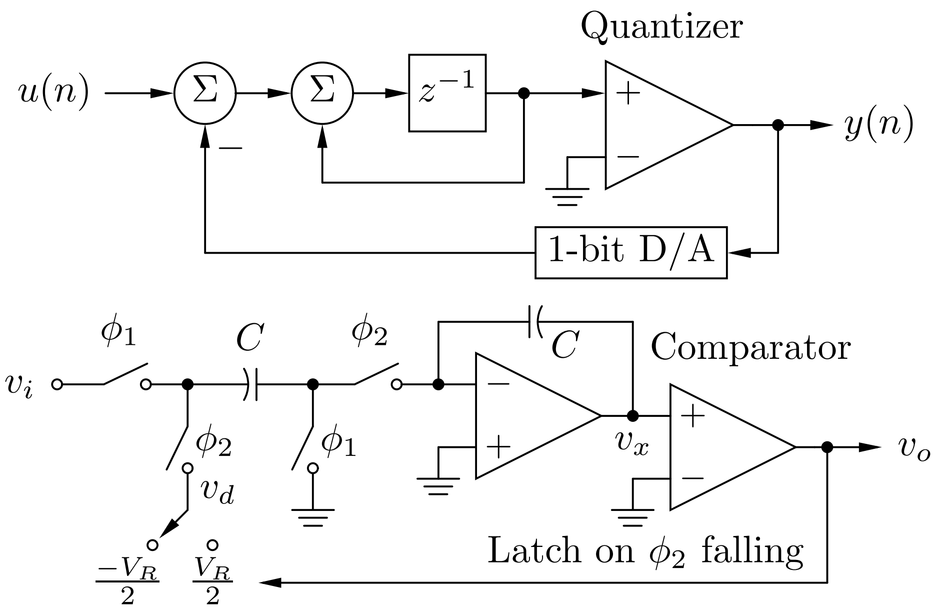
- Maximum SNR: $\sin(\pi f/f_s) \simeq \pi f/f_s$ for $f_0 \ll f_s$.

$$P_n = \int_{-f_0}^{f_0} S_n^2(f)|N(f)|^2 df \simeq \frac{\Delta^2 \pi^2}{36}\left(\frac{1}{\mathrm{OSR}}\right)^3$$

$$\therefore \mathrm{SNR}_{\max} = 6.02\mathrm{N} + 1.76 - 5.17 + 30\log(\mathrm{OSR}) \rightarrow 1.5 \text{ bits/octave}$$

Realization of A First-Order ΔΣ Modulator

❑ First-order ΔΣ modulator and SC implementation.



Second-Order Noise Shaping

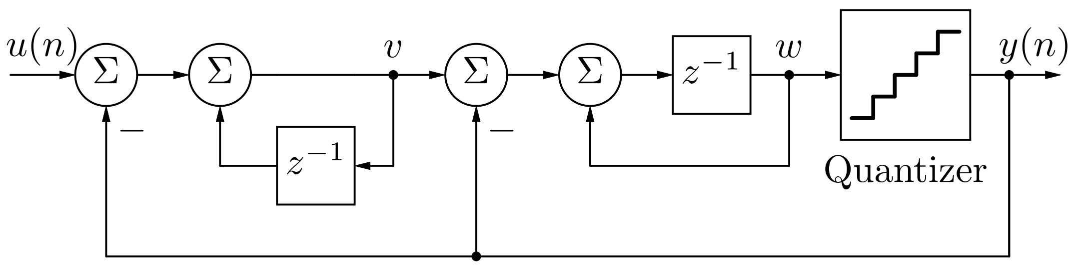
❑ Transfer function: linear quantizer model.

$$U - Y + Vz^{-1} = V, \quad (V - Y + W)z^{-1} = W$$

$$Y(z) = W + E = z^{-1}U(z) + (1 - z^{-1})^2 E(z)$$

$$\therefore S(z) = z^{-1}, \quad N(z) = (1 - z^{-1})^2$$

❑ Second-order ΔΣ modulator.

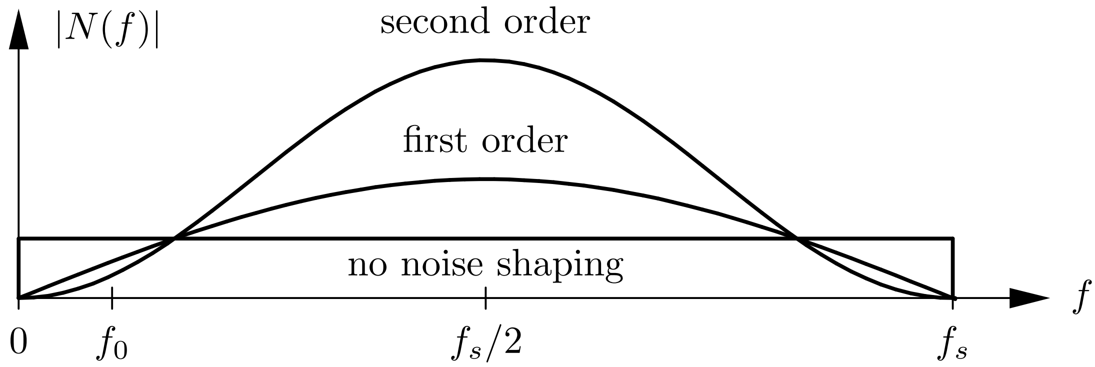


❏ Maximum SNR: $z = e^{j\omega T} = e^{j2\pi f/f_s}$, $\sin(\pi f/f_s) \simeq \pi f/f_s$ for $f_0 \ll f_s$.

$$|N(f)| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2, \quad P_n \simeq \frac{\Delta^2\pi^4}{60}\left(\frac{1}{\text{OSR}}\right)^5$$

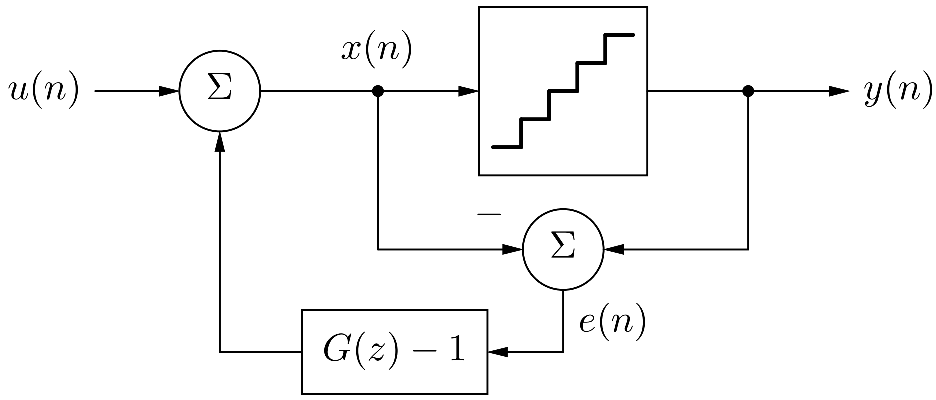
$$\therefore \text{SNR}_{\text{max}} = 6.02\text{N} + 1.76 - 12.9 + 50\log(\text{OSR}) \rightarrow 2.5 \text{ bits/octave}$$

❏ Noise transfer-function curves: P_n in the signal band (0 to f_0).



Error-Feedback Structure

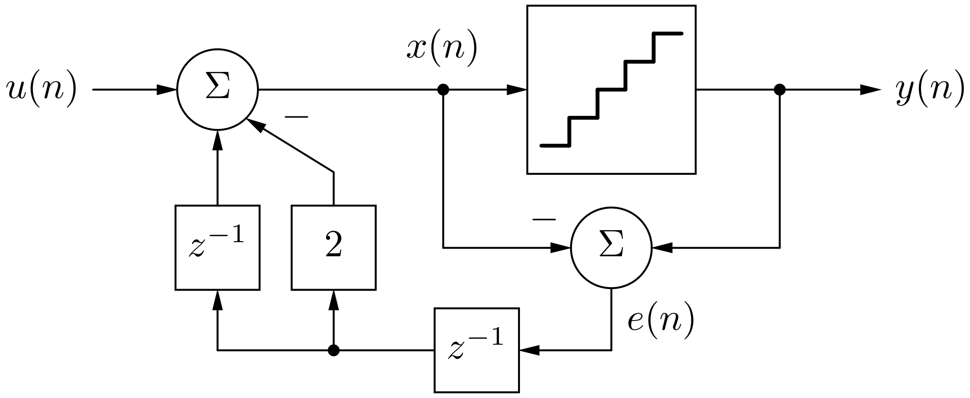
❏ Error-feedback structure of a general ΔΣ modulator.



❏ Transfer function for a first-order modulator.

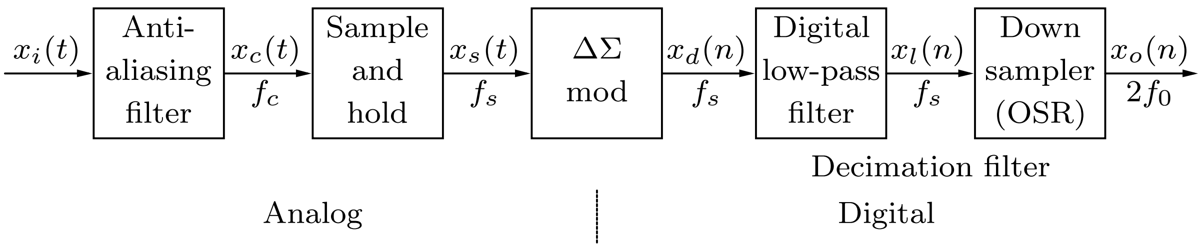
$$Y(z) = U(z) + G(z)E(z), \quad S(z) = 1, \quad N(z) = G(z) = 1 - z^{-1}$$

- ❑ Mismatches of the analog subtracters → significant noise-shaping degradation. For example, if the subtraction becomes $e = y - 0.99x$ rather than $e = y - x$, then $N(z) = 1 - 0.99z^{-1}$, and the zero is moved off dc. → The noise is not fully nulled at dc. → Well suited to *digital implementations* where no coefficient mismatches occur.
- ❑ Error-feedback structure of a 2nd-order $\Delta\Sigma$: $G(z) = (1 - z^{-1})^2$.

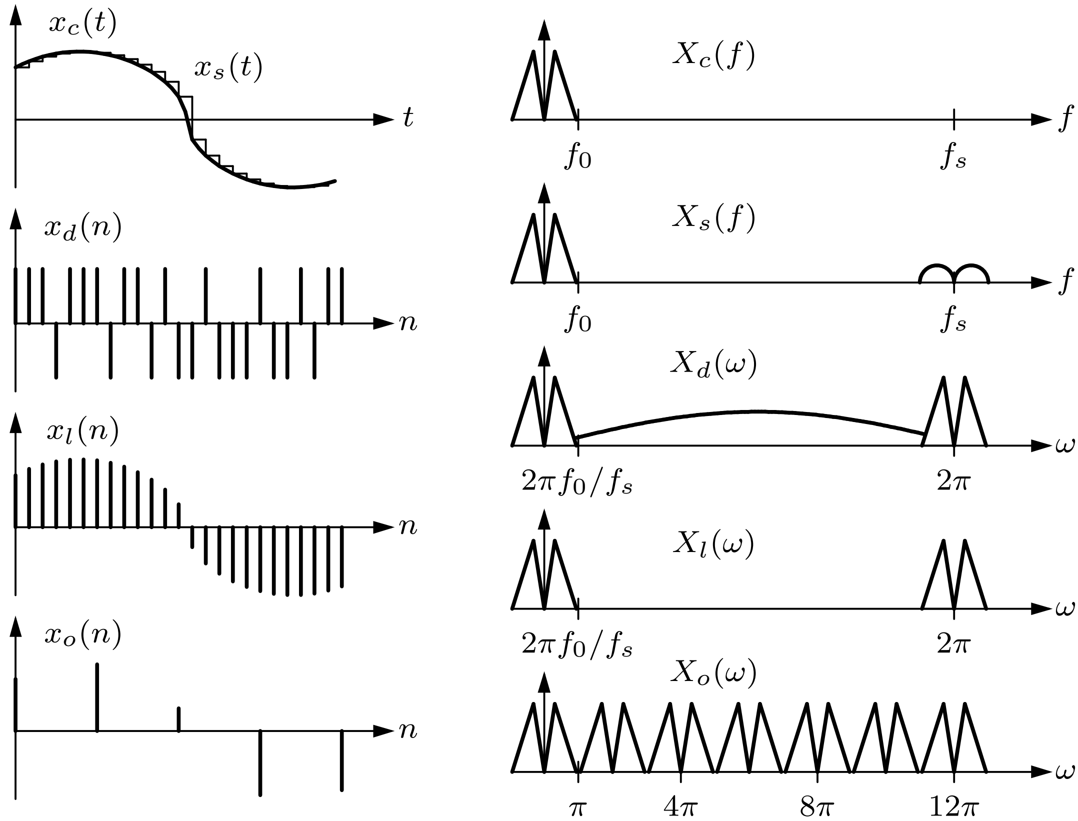


System Architecture of Delta-Sigma ADCs

- ❑ System architecture for a typical $\Delta\Sigma$ oversampling ADC.

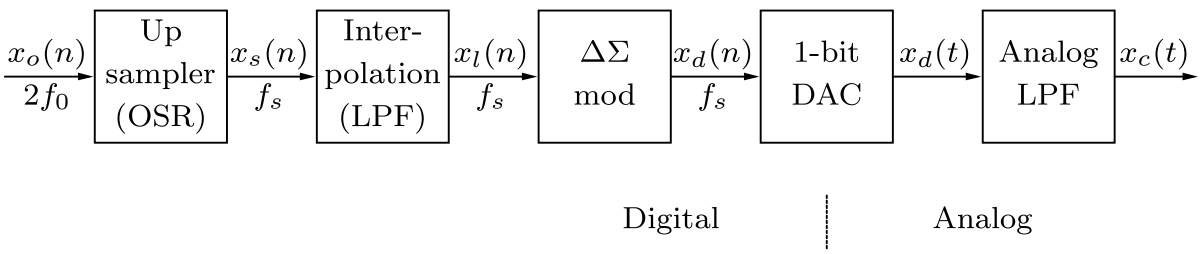


- ❑ Antialiasing filter having cutoff frequency $f_c \le f_s/2$, S/H having $\sin x/x$ response, 1-bit $\Delta\Sigma$ modulator having output levels of ± 1, digital LPF having cutoff frequency $f_c = 2f_0$ (to remove out-of-band quantization noise), decimation process by resampling at $2f_0$.
- ❑ Signals and spectra in oversampling ADCs.



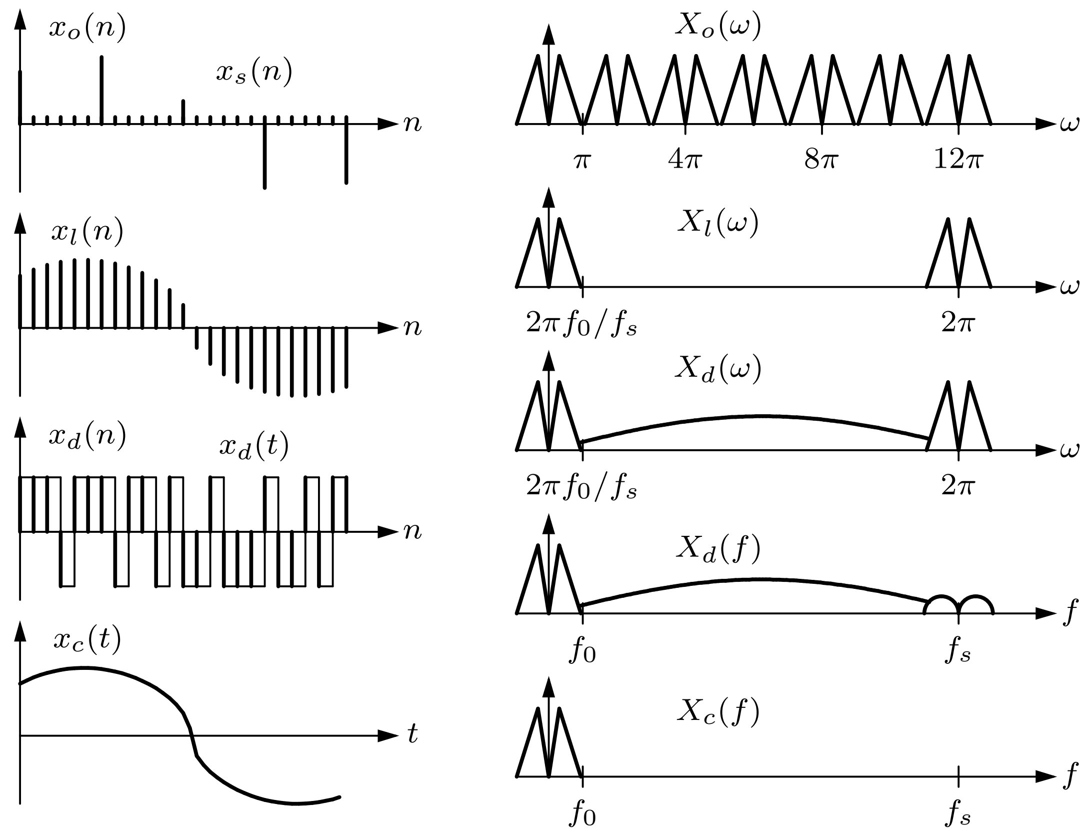
System Architecture of Delta-Sigma DACs

- System architecture for a 1-bit $\Delta\Sigma$ oversampling DAC.



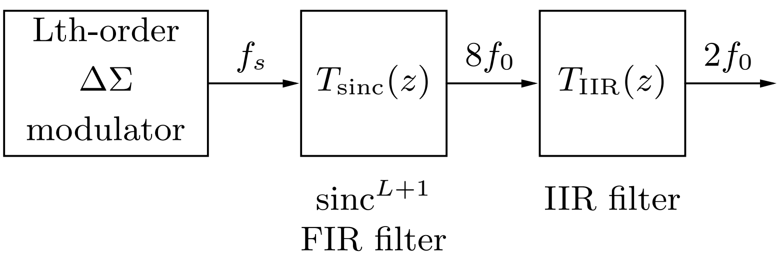
- f_0 is slightly greater than the highest input frequency, an *interpolation filter* is used to create the multibit digital signal by digitally filtering out the images ($f_c = f_0$), a fully digital $\Delta\Sigma$ modulator for noise shaping, a 1-bit DAC with excellent linearity, an analog filter to filter out out-of-band quantization noise.

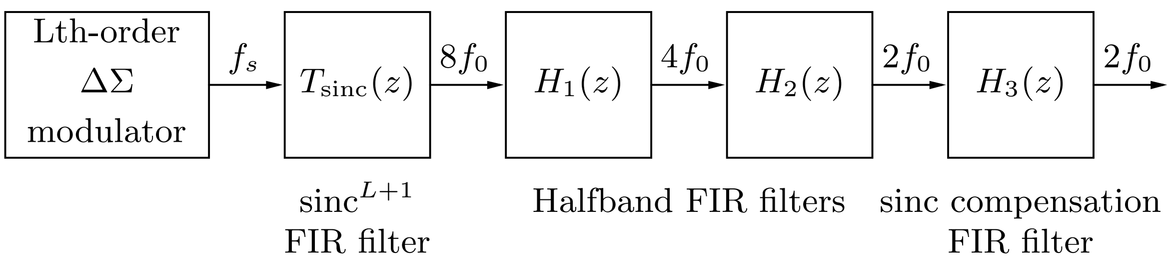
- Signals and spectra in oversampling DACs.



Digital Decimation Filters

❑ *Multistage*: an FIR filter + an IIR filter or a cascade of FIR filters.





❏ The sinc^{L+1} FIR filter: a cascade of $L+1$ *averaging filters*, transfer function $T_{\text{avg}}(z)$ of an averaging filter, decimation ratio $M = f_s/8f_0$.

$$T_{\text{avg}}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i}$$

❏ An example of averaging filters for noise reduction: $M = 4$.

$$\text{1-bit signal} = \{1,\ 1,\ -1,\ 1,\ 1,\ -1,\ 1,\ 1,\ -1,\cdots\}$$
$$x_{lp1}(n) = \{0.5,\ 0.5,\ 0.0,\ 0.5,\ 0.5,\ 0.0,\cdots\}$$
$$x_{lp2}(n) = \{0.375,\ 0.375,\ 0.25,\ 0.375,\ 0.375,\ 0.25,\cdots\}$$
$$x_{lp3}(n) = \{0.344,\ 0.344,\ 0.313,\ 0.344,\ 0.344,\ 0.313,\cdots\}$$

❏ Halfband FIR filters: passband from 0 to $\pi/2$, stopband from $\pi/2$ to π, every second coefficient $= 0$, downsampling by 2.

❏ Frequency response of an averaging filter.

$$\begin{aligned} MY(z) &= \sum_{i=0}^{M-1} z^{-i}U(z) = (1 + z^{-1} + z^{-2} + \cdots + z^{-(M-1)})U(z) \\ &= (z^{-1} + z^{-2} + \cdots + z^{-M})U(z) + (1 - z^{-M})U(z) \\ &= MY(z)z^{-1} + (1 - z^{-M})U(z) \end{aligned}$$

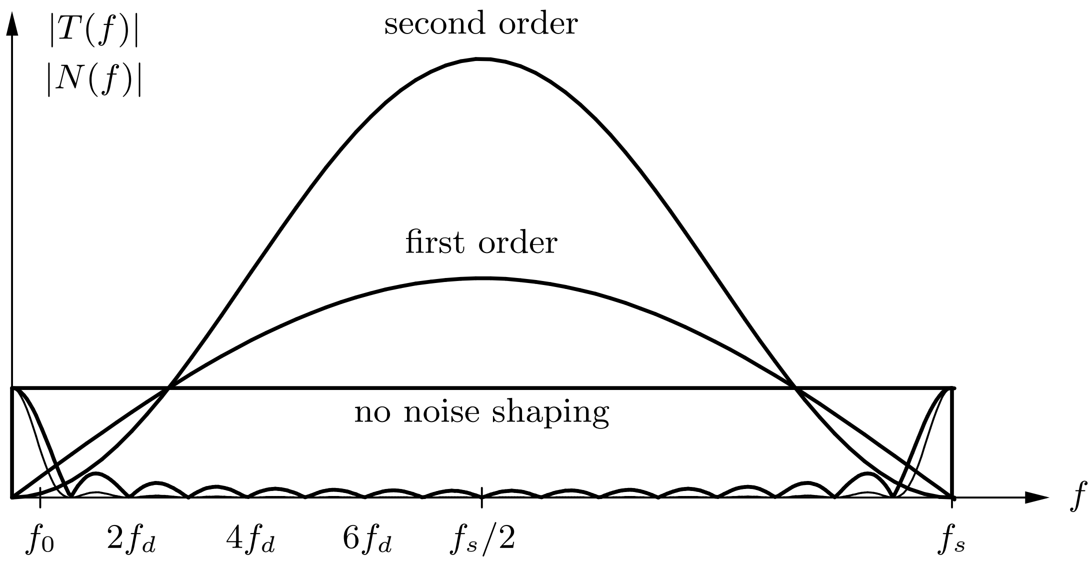
$$\therefore T_{\text{avg}}(z) = \frac{Y(z)}{U(z)} = \frac{1}{M}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right), \quad |T_{\text{avg}}(e^{j\omega})| = \frac{\text{sinc}(\omega M/2)}{M\text{sinc}(\omega/2)}$$

❏ Frequency response of cascaded $L+1$ averaging filters: The order of this low-pass filter should be *one more* than the order L of $\Delta\Sigma$ modulation (attenuation slope of filter $>$ rising slope of noise).

$$T_{\text{sinc}}(z) = \frac{1}{M^{L+1}}\left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{L+1}$$

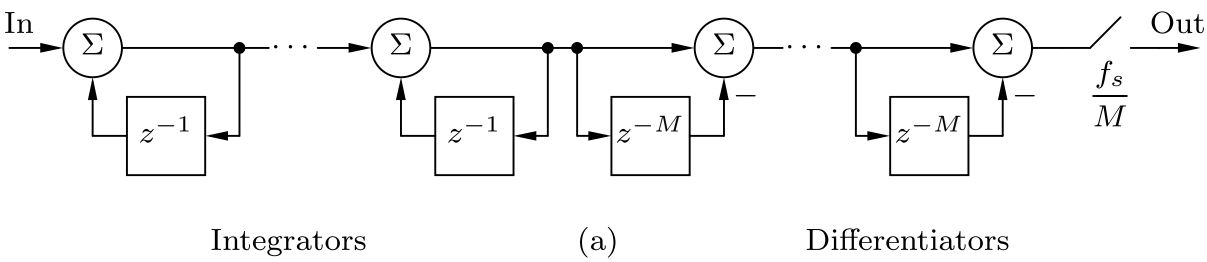
Frequency Response of sinc Filters

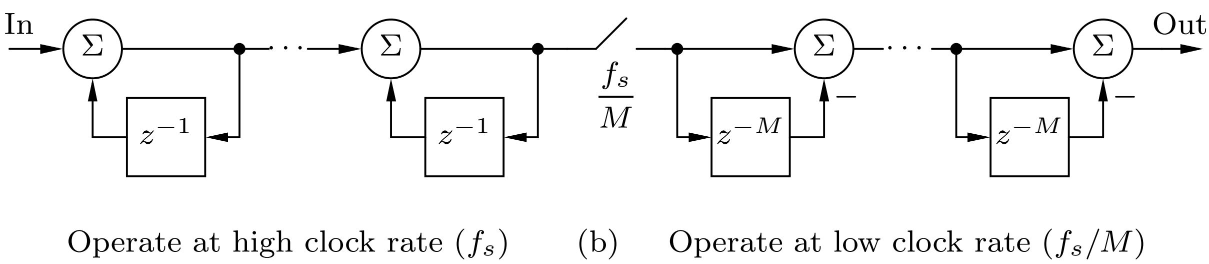
❏ Signal band from 0 to f_0, decimation frequency f_d, sampling frequency f_s, $f_d = f_s/16$, sinc^1 and sinc^2 filters.



❏ Realizing $T_{\mathrm{sinc}}(z)$ as a cascade of integrators and differentiators, (a) downsampling *after* filtering, (b) a more efficient method.

$$T_{\mathrm{sinc}}(z) = \frac{1}{M^{L+1}} \left(\frac{1}{1 - z^{-1}} \right)^{L+1} \left(1 - z^{-M}\right)^{L+1}$$





❏ Purpose of an IIR filter or a cascade of FIR filters: to remove any HF input signals (sharp anti-aliasing filter), to compensate for the droop in the passband by the $T_{\text{sinc}}(z)$ filter (sinc-compensation filter).

❏ *Single stage*: a relatively high-order FIR filter.

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

For example, a 2048 tap FIR filter was used to decimate 1-bit stereo outputs from two $\Delta\Sigma$ modulators having OSR of 64. The output need only be calculated at the Nyquist rate such that 2048 additions are required during one clock cycle. If the Nyquist rate is 48 kHz, the single accumulator would have to be clocked at 98.3 MHz (2048 × 48 kHz). To overcome this high clock rate, 32 separate FIR filters are realized with shared coefficients in a time-interleaved fashion.
→ 32 FIR filters operating at 3 MHz (2048 × 48 kHz / 32).

High-Order Modulators

❏ Noise transfer function for an Lth-order noise-shaping modulator.

$$N(z) = (1 - z^{-1})^L$$

❏ Maximum SNR: $z = e^{j\omega T} = e^{j2\pi f/f_s}$, $\sin(\pi f/f_s) \simeq \pi f/f_s$ for $f_0 \ll f_s$.

$$|N(f)| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L, \quad P_n \simeq \frac{\Delta^2 \pi^{2L}}{12(2L+1)}\left(\frac{1}{\text{OSR}}\right)^{2L+1}$$

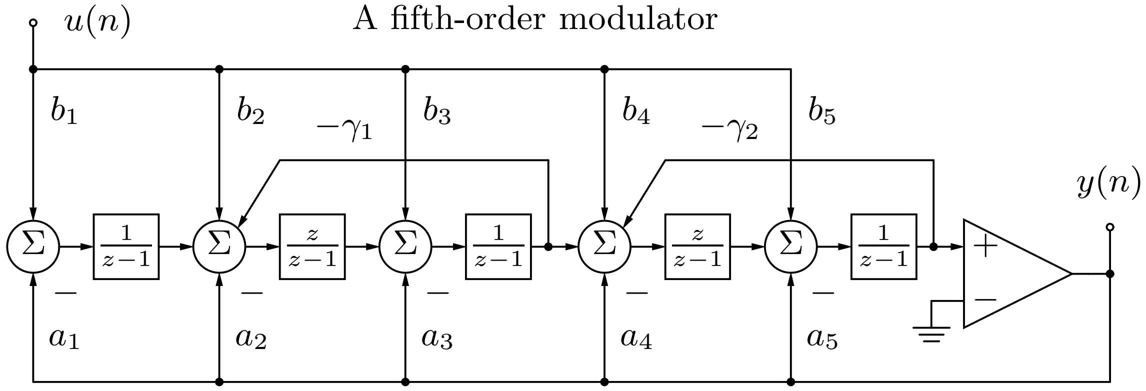
$$\therefore \text{SNR}_{\text{max}} = 6.02\text{N} + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + 10\log\left(\text{OSR}^{2L+1}\right)$$

improves SNR by $3(2L+1)$ dB/octave or $(L+0.5)$ bits/octave.

Interpolative Architecture

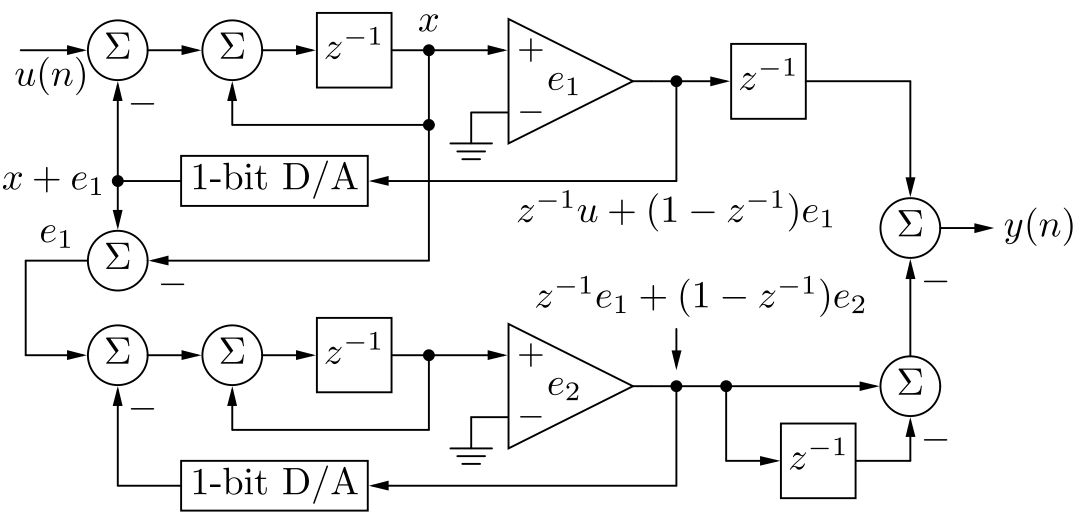
- Reduced component sensitivity but instability for large input signals.
- Chain of integrators with weighted feedforward summation, chain of integrators with feedforward summation and local resonator feedbacks.
- Chain of integrators with distributed feedback (a_i), distributed feedforward (b_i), and local resonator feedbacks ($-\gamma_i$): a_i, $a_i + b_i$, or $a_i + b_i + \gamma_i$.

A fifth-order modulator



Multistage Noise Shaping Architecture

- Cascade of lower-order single-loop modulators, MASH (MultistAge noise SHaping). Since the lower-order modulators are *more stable*, the overall system should remain stable.



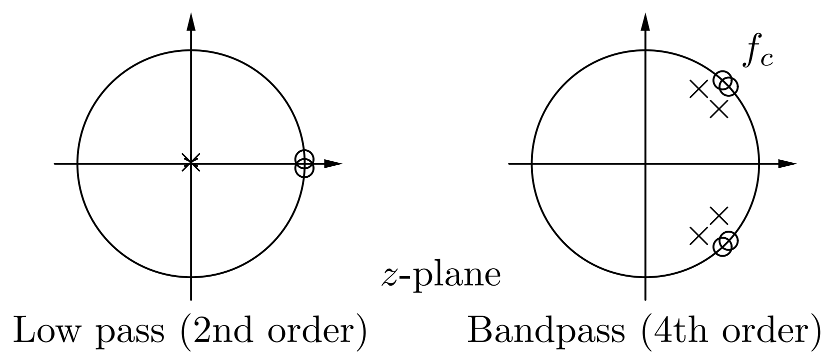
- A second-order MASH modulator using two first-order modulators.
- Signal and noise transfer functions: e_1 is removed completely.

$$Y(z) = z^{-2}U(z) - (1 - z^{-1})^2 E_2(z)$$

- MASH approaches are *sensitive* to finite opamp gain and mismatches between analog and digital circuitry. → First-order noise leakage → To alleviate the mismatch problem, the first stage is chosen to be a higher-order modulator. → Any noise leakage does not have as serious an effect as 1st-order noise leakage.
- Note that the output $y(n)$ is a four-level signal due to the combination of the original two-level signals. → Require a linear four-level D/A converter for D/A applications, a more complex FIR decimation filter for A/D applications.

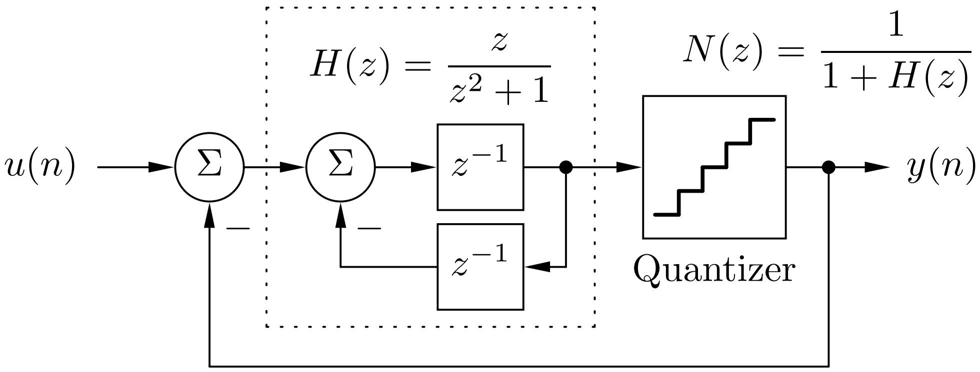
Bandpass Oversampling Converters

- *Band-reject noise shaping* for narrow-band signals: digital radios.
- $H(z)$ has high gain but $N(z)$ is small near the center frequency f_c. → $H(z)$ is a resonator that has poles near $z = e^{\pm j2\pi f_c/f_s}$.
- Oversampling ratio OSR = $f_s/2f_b$: f_b = signal bandwidth.
- The pole and zero locations of noise transfer functions: $(1 - z^{-1})^2$



A Bandpass Oversampling Modulator

- Transfer function of a 2nd-order bandpass integrator: poles at $\pm j$.
- Noise transfer function: *only one zero* at j, another zero at $-j$.
- SNR improvement of 1.5 bits/octave equals that of a first-order low-pass modulator with only one zero at dc.



Stability for ΔΣ Modulators

- A stable modulator: the input to the quantizer remains *bounded.*
- An *overloaded* quantizer: the input goes beyond the quantizer's normal range. ← instability by feedback
- The stability of higher-order 1-bit modulators is not well understood because of a highly nonlinear quantizer. → stable for one input but unstable for another → *absence of a rigorous theory* for stability
- A general rule of thumb for stability: 1-bit quantizer, poles of $N(z)$.

$$|N(e^{j\omega})| \leq 1.5 \quad \text{for } 0 \leq \omega \leq \pi$$

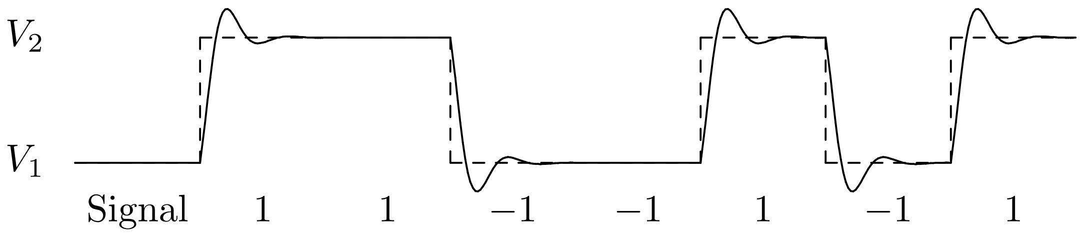
- The stability is also related to the maximum input signal level.
- Circuitry for detecting and recovering instability (long strings of 1s or 0s, large signal amplitude), multibit DAC for improving stability.

Linearity of Two-Level Converters

❑ 1-bit D/A converters are *inherently linear* because of having only two output levels to define a straight line. But practical issues limit this linearity. Most of these issues are applicable to multibit converters.

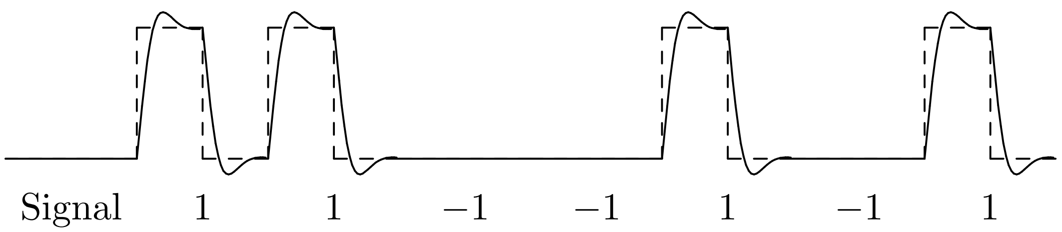
❑ Two output levels are *related* to power supply voltages (LF drift). The clock feedthrough and jitter is dependent on supply voltages.

❑ There is *memory* between output levels of NRZ coding. One way for high linearity is to *match* falling and rising signals (difficult task).



❑ A better way to obtain high linearity without matching falling and rising signals is to use some sort of *memoryless coding scheme*.

❑ A RTZ coding scheme.



❑ Other memoryless scheme: using two levels of opposite signs but ensuring that the signal settles to ground between samples.

❑ Switched-capacitor circuits implement memoryless coding since capacitors are *charged* on one clock phase and *discharged* on the next. → Most oversampling ADCs are realized using SC circuits.

Idle Tones

❏ A signal with dc level of 1/3 applied to a first-order ΔΣ modulator having a 1-bit quantizer with output levels of ±1. The output will be a sequence with the period of 3 cycles.

$$y(n) = \{1, -1, 1, 1, -1, 1, 1, -1, \ldots\}$$

The output power is concentrated at dc and $f_s/3$. For OSR of 8, the post low-pass filter ($f_0 = f_s/16$) will eliminate the HF content such that only the dc level of 1/3 remains.

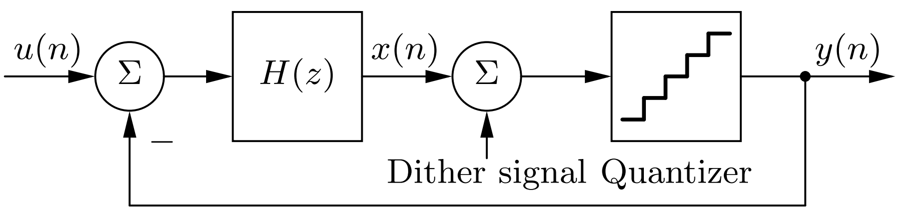
❏ A signal with dc level of $(1/3 + 1/24) = 3/8$. The output will be a sequence with the period of 16 cycles and has *some power* at $f_s/16$.

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, \ldots\}$$

The signal power at $f_s/16$ will *not* be filtered out. → *idle tones*.

Dithering

❏ Act of introducing some *random signal* into a modulator to *reduce* the amount of idle tones. For noise shaping of dithering signal, the most suitable place to add dithering signal is *just before* the quantizer.



❏ The dithering signal is realized using a pseudo-random number generator with only a few bits of resolution.

❏ Since the power of dithering signal is *similar* to the quantization noise power, the use of dithering *adds* about 3 dB extra inband noise and often requires *rechecking* the stability.

Finite Opamp Gain

- Transfer function of a switched-capacitor integrator (noninverting) with a finite opamp gain A. Assume $C_1 \simeq C_2$ for typical converters.

$$v_x(n) = v_{C2}(n) - v_x(n)/A \quad \text{(1st-order modulator)}$$

$$C_2[v_{C2}(n) - v_{C2}(n-1)] = C_1[v_i(n-1) - v_x(n)/A]$$

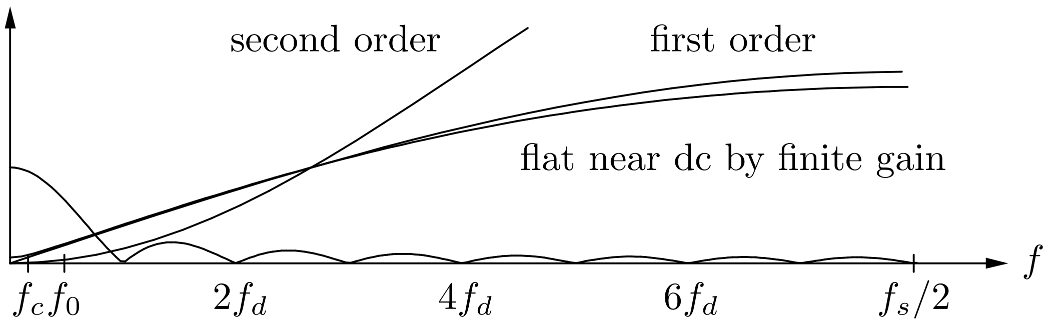
$$H(z) = \frac{C_1/C_2}{(1+1/A+C_1/C_2A)z - (1+1/A)} \simeq \frac{(1+2/A)^{-1}}{z-(1-1/A)}$$

The pole (zero of N) *moves* to the left of $z=1$ by an amount $1/A$.

- Noise transfer function: does *not* have a zero at dc ($z=1$).

$$N(z) = \frac{1}{1+H(z)} = \left.\frac{z-(A+1)/(A+2)}{z-1/(A+2)}\right|_{z=1} = \frac{1}{A+1}$$

- The quantization noise is *flat* below the break frequency $f_c \simeq f_s/2\pi A$.



- The signal band f_0 should be *greater* than f_c to obtain noise-shaping benefits for any further increasing OSR. Designers will typically ensure that the opamp gain is at least *twice* the oversampling ratio.

$$f_0 > f_s/2\pi A, \quad \therefore A = 2 \times \text{OSR} > \text{OSR}/\pi$$

- The above analysis *only* applies for modulators having a *single* D/A feedback, and does not apply to MASH or cascade modulators, where larger opamp gains are often required to match analog/digital paths.

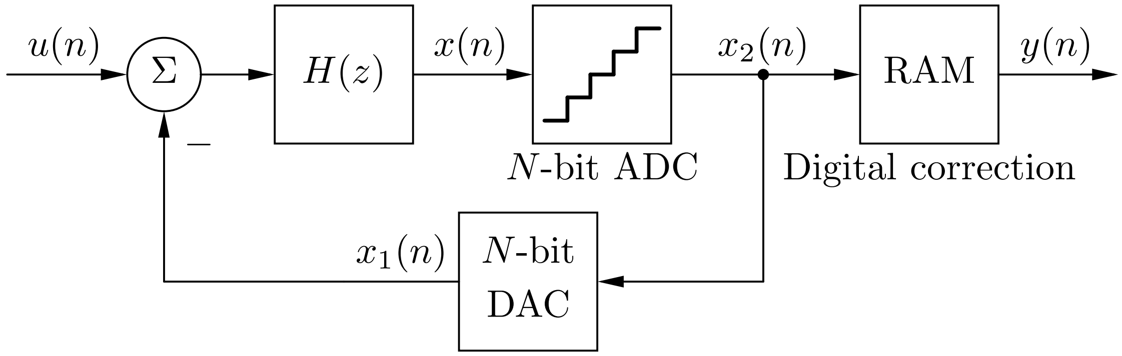
Multibit Oversampling Converters

- 1-bit oversampling converters: highly linear data conversion without precision component matching, instability due to the high degree of nonlinearity in the feedback, existence of idle tones, high-order analog filtering due to substantial out-of-band quantization noise power.
- *Multibit* oversampling converters: *reduction* of quantization noise power by 6 dB/bit, extra resolution without increasing OSR, high speed and low power operation due to lower sample rate, *reduced* linearity and more analog circuitry, M-bit quantizer, M-bit DAC ($2 \sim 4$ bits are typical).

DAC Architectures for Improved Linearity

- Multibit randomizer D/A converter: element mismatch is converted from a dc error into a wide-band mismatch noise by *randomly* choosing different elements (resistors, capacitors, current sources) to represent a digital input code at different times. → *dynamic element matching* → A multibit oversampling DAC had 15-bit linearity for peak element mismatches of 0.2%.
- Dynamic matched current sources in a D/A converter: each current source is periodically *calibrated* with a single reference current source through the use of a shift register, MOSTs, and switches. → effective dynamic range of 90 – 115 dB (15 – 20 bits).

- Digital calibration A/D converter: a 2^N-word look-up RAM contains the accurate digital *equivalents* of actual output levels of the nonlinear N-bit DAC for $x_2(n)$, $y(n) = x_1(n) \simeq u(n)$, calibration cycle.



- ADC with *both* multibit and single-bit feedback: the multibit quantizer is used to *cancel* the large quantization error due to the 1-bit quantizer, high-order noise shaping for the quantization error due to the multibit quantizer and the nonlinearity of the multibit DAC → *dual-quantizer* ADC architectures.

- A switched-capacitor 3rd-order ΔΣ modulator.

Homework

- Modeling of first-order ΔΣ modulators by the C language.
- Problems 14.1, 14.2, 14.3, 14.4, 14.5, 14.8.

References

[1] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation*, IEEE Press, New York, 1997.

[2] S. Rabii and B. A. Wooley, *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators*, Kluwer Academic Publishers, The Netherlands, 1999.