Nyquist-Rate D/A Converters

劉 尙 大 敎授

전 자 공 학 부

Kyungpook National University

Nyquist-Rate CMOS D/A Converters

- ❏ Decoder-based DAC.
- ❏ Binary-scaled DAC.
- ❏ Thermometer-code DAC.
- ❏ Hybrid DAC.
- ❏ Oversampling DAC.

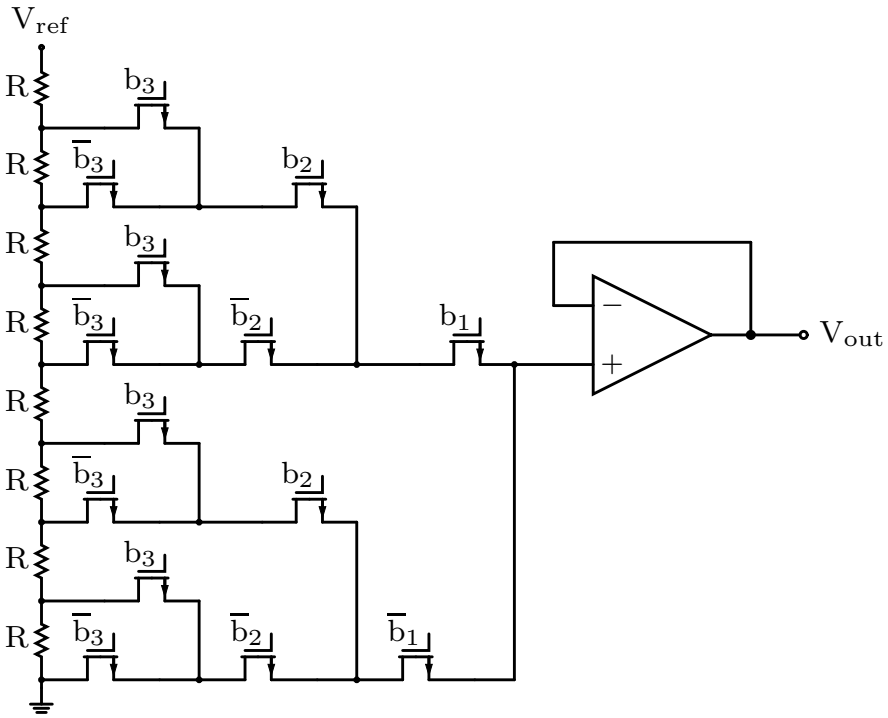
Decoder-Based D/A Converters

- Create 2^N reference signals using resistor strings.
- Pass the appropriate reference signals to the output through switches by the digital input.
- Resistor-string D/A converters.
- Folded resistor-string D/A converters.
- Multiple R-string D/A converters.

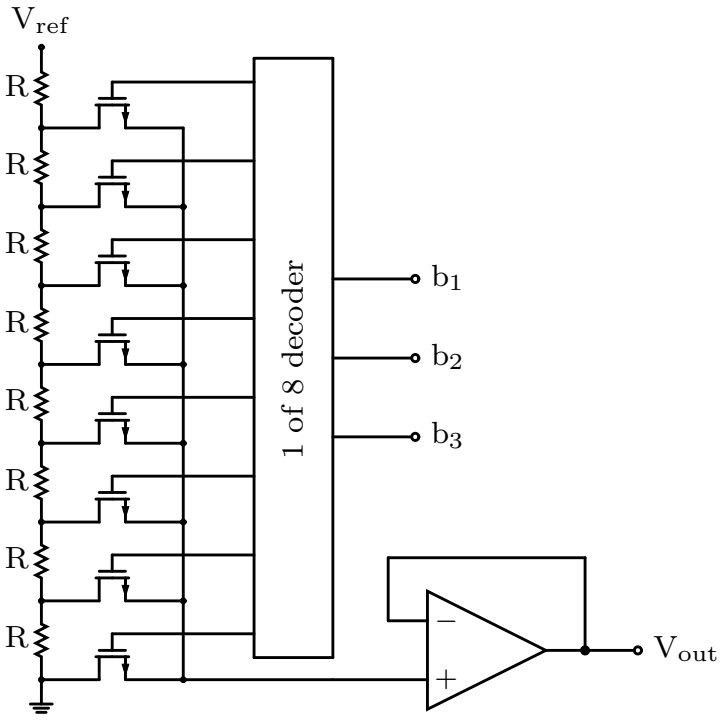
Resistor-String D/A Converters

- One of the first integrated MOS 8-bit DAC.
- Switch = pass transistor or CMOS transmission gate.
- Accuracy ⇐ matching precision of R
  Polysilicon resistor ⇒ 20 ∼ 30 Ω/□, 10-bit accuracy.
- Guaranteed monotonicity for voltage-insensitive V_{OS} of the buffer.
- Delay through the switch network: $\tau \approx RCn^2/2 = \sum R_{oi}C_i$.
- Tree decoding or digital decoding (2^N junctions on the output line).

❑ Resistor-string 3-bit D/A converter with tree decoding.

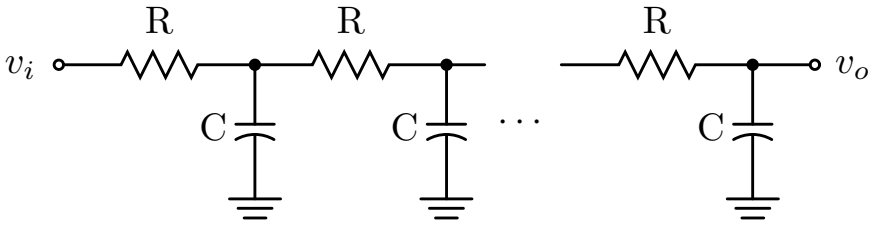


❑ Resistor-string 3-bit D/A converter with digital decoding.



Delay through Switch Network or Resistor String

❑ Estimating the time constant for n resistors and capacitors



❑ Open-circuit time-constant approach ($v_i = 0$)

$$\tau \approx \sum_{i=1}^{n} R_{oi}C_i = RC + 2RC + \cdots + nRC = \frac{n(n+1)RC}{2} \simeq \frac{n^2}{2}RC$$

❑ Output voltage: settling time $t_s = 7\tau$ for v_o to equal 0.999 V

$$v_i = u(t), \quad v_o \simeq 1 - e^{-t/\tau}$$

Folded Resistor-String Converters

❑ Decoding similar to that for a digital memory:
word lines, bit lines.

❑ Reduction in digital decoding area.

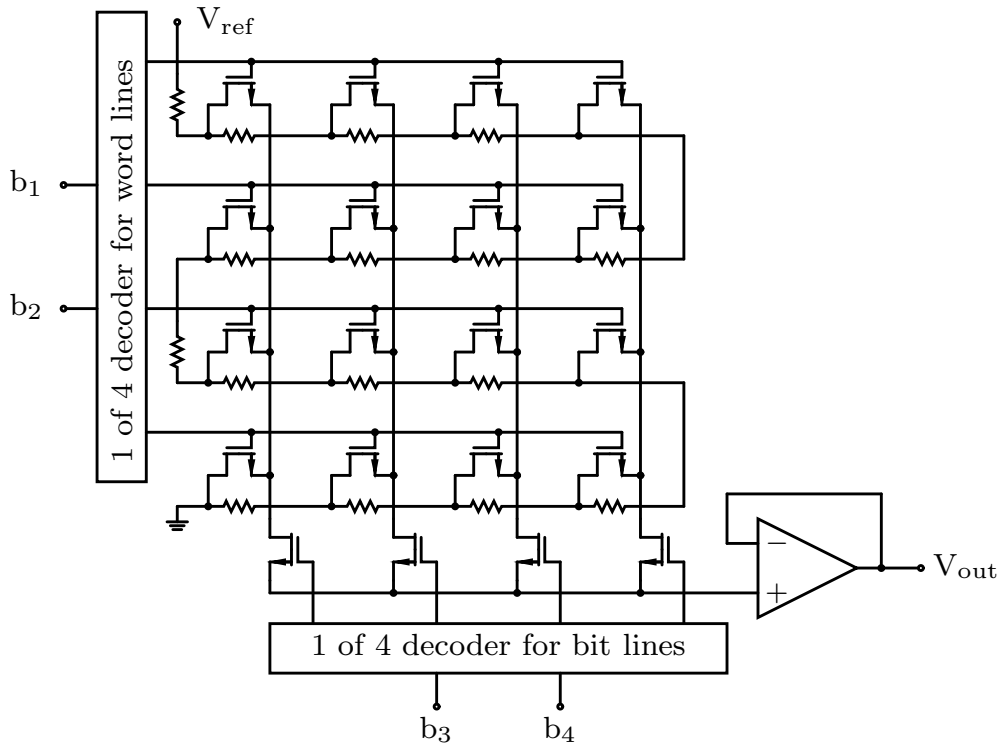
❑ Reduction of capacitive loading.

❑ Number of transistor junctions on the output line = $2\sqrt{2^N}$.

❑ Increase in speed.

❑ Guaranteed monotonicity for voltage-insensitive V_{OS}.

❑ A 4-bit folded resistor-string D/A converters.



Multiple R-String Converters

❑ Number of resistors $= 2 \times 2^{N/2} < 2^N$.

❑ Higher-resolution and low-power applications.

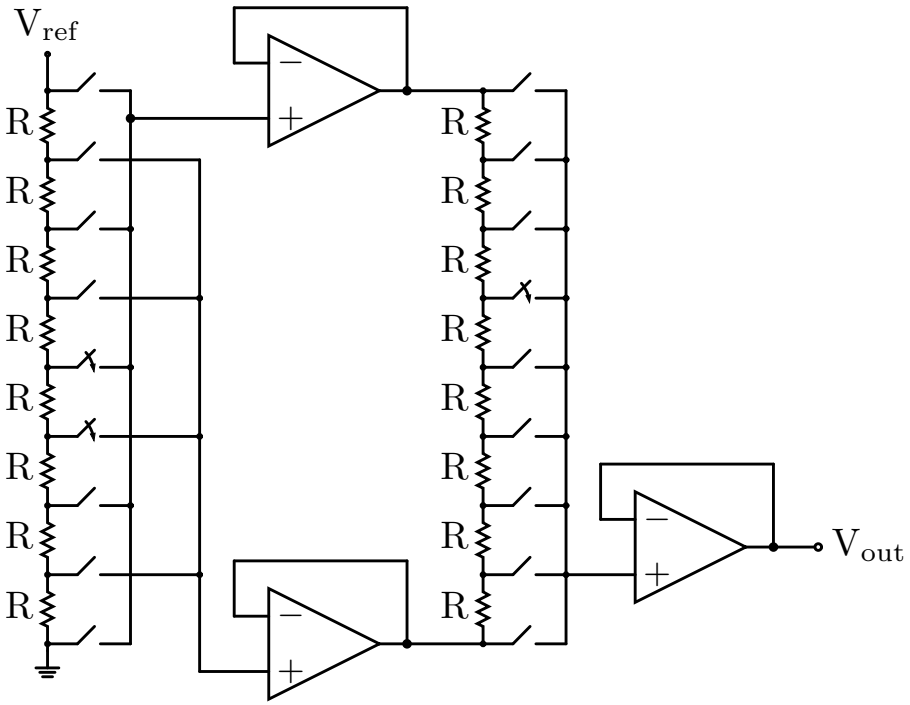
❑ The second resistor string linearly interpolates between the two adjacent voltages from the first resistor string.

❑ Not-severe matching requirements for the second resistor string (lower-order bits).

❑ Extra logic to make the top buffer has the higher voltage.

❑ Guaranteed monotonicity for matched opamps and voltage-insensitive V_{OS}.

❑ A 6-bit multiple R-string D/A converters.



Binary-Scaled Converters

❑ The most popular approach.

❑ Combining binary-weighted signals = current or charge.

❑ Binary-weighted resistor converters.

❑ R-2R-based converters.

❑ Switched-capacitor D/A converters.

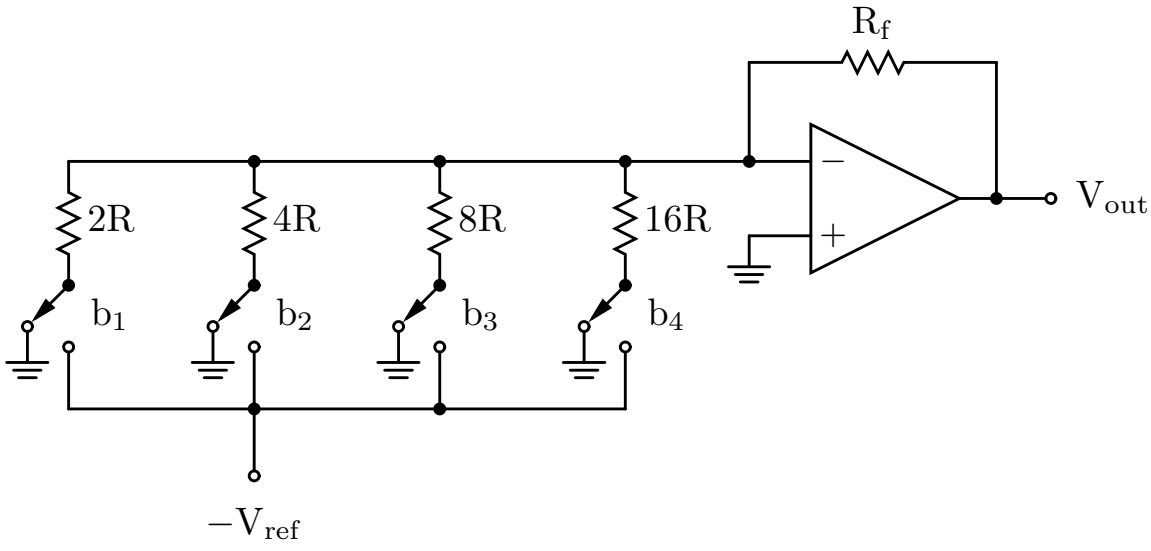
❑ Current-mode converters.

Binary-Weighted Resistor Converters

- ❏ Popular for bipolar technology.
- ❏ Number of resistors = $N \ll 2^N$.
- ❏ Large resistance and current ratios = 2^N.
- ❏ Scaled switches for large current ratios.
- ❏ No guarantee of monotonicity.
- ❏ Glitches in high-speed operation.

$$V_{out} = -R_f V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \frac{b_4}{16R}\right) = \frac{R_f}{R} V_{ref} B_{in}$$

- ❏ Binary-weighted 4-bit resistor D/A converters.

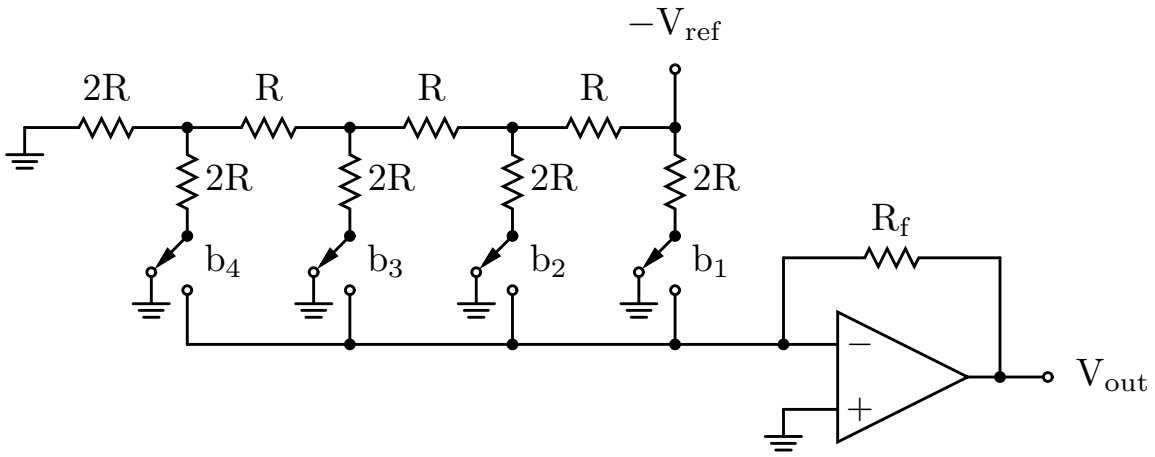


R-2R-Based Converters

- ❏ Very popular architecture.
- ❏ Binary-weighted currents by R-2R ladder.
- ❏ Number of resistors = $2N \ll 2^N$.
- ❏ Small resistance ratio = $2 \ll 2^N$: independent of N.
- ❏ $R = 2 \sim 10$ kΩ, $2R = R + R$ to improve matching.
- ❏ Scaled switches for large current ratios: $1/2 \sim 1/2^N$.

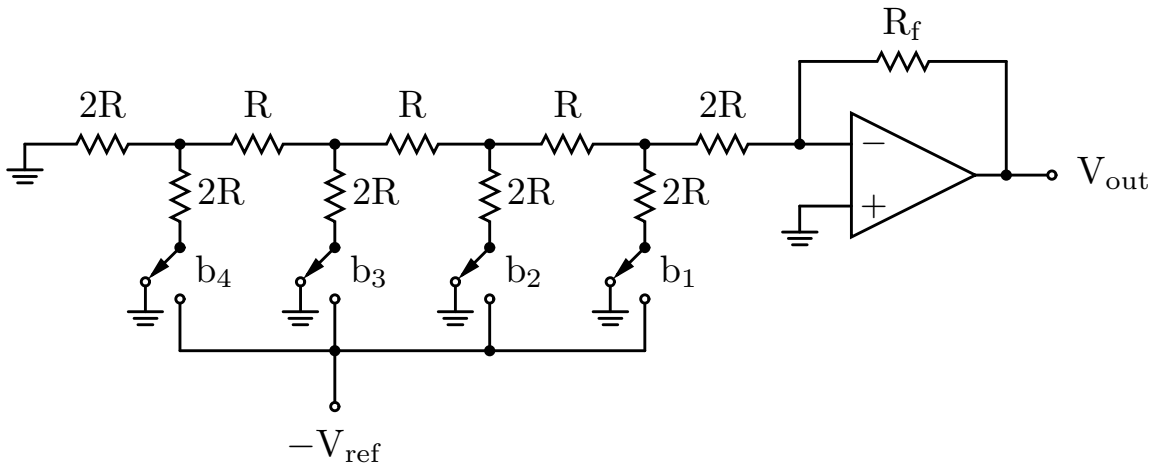
- ❏ Current-driven converter: inverted R-2R ladder.

$$V_{out} = -R_f \frac{V_{ref}}{R}\left(-\frac{b_1}{2} - \frac{b_2}{4} - \frac{b_3}{8} - \frac{b_4}{16}\right) = \frac{R_f}{R} V_{ref} B_{in}$$



❏ Voltage-driven converter: 4-bit R-2R based DAC.

$$V_{out} = -R_f \frac{V_{ref}}{3R}\left(-\frac{b_1}{2} - \frac{b_2}{4} - \frac{b_3}{8} - \frac{b_4}{16}\right) = \frac{R_f}{3R} V_{ref} B_{in}$$



Switched-Capacitor D/A Converters

❏ SC gain amplifier + programmable capacitor array (PCA)

❏ Weighted-capacitor DAC: $V_{out} \propto V_{ref} B_{in} \rightarrow V_{in} B_{in}$ (multiplying).

❏ Insensitive to offset voltage, 1/f noise, and finite gain.

❏ Two (N/2)-bit PCAs for large N: requires an extra opamp.

❏ Bottom plate never be connected to the inverting input of opamp.

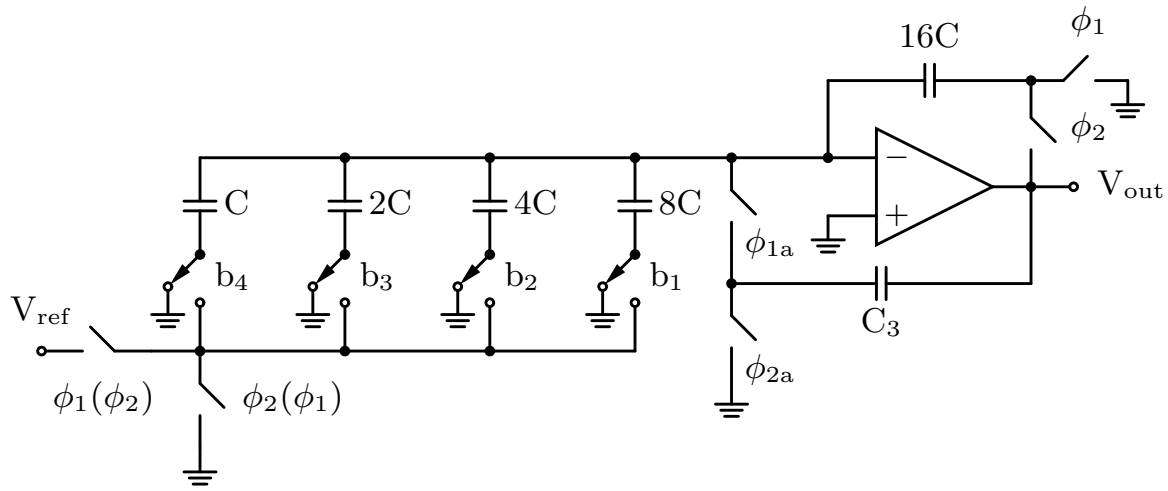
❏ PCA programming time to reduce noise: when no potentials are altered by switching, or no signals are being processed.

❏ PCA connection method for easy compensation: a constant capacitive load at the input terminal of the opamp.

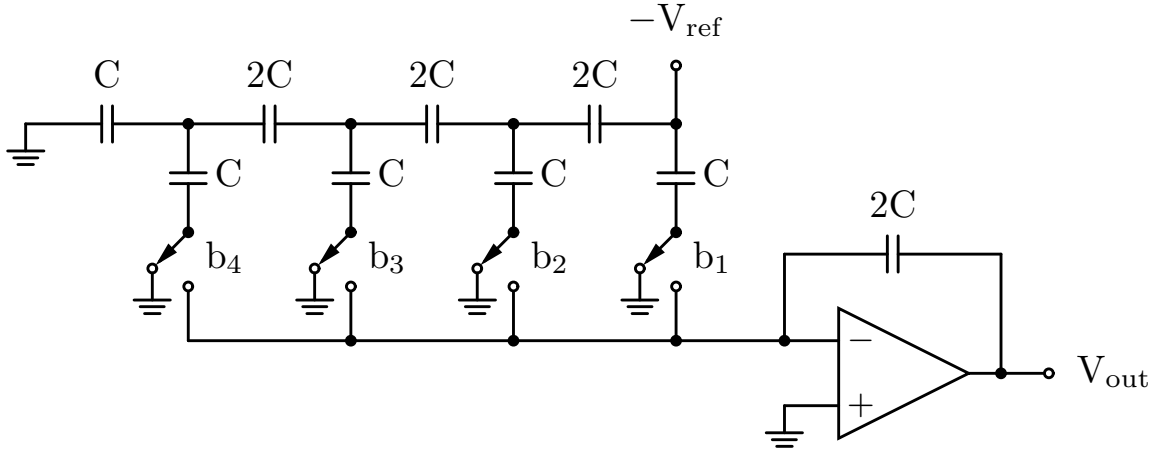
❏ Binary-array charge-redistribution D/A converter.

❏ Noninverting (inverting), capacitive-reset gain (C_3), deglitching capacitor (C_4) for continuous-time feedback (all switches open).

$$C(V_{ref} - V_{OS}) - 16CV_{OS} = -CV_{OS} + 16C(V_{out} - V_{OS}), \quad \therefore V_{out} = \frac{1}{16}V_{ref}$$



❏ C-2C ladder D/A converter.



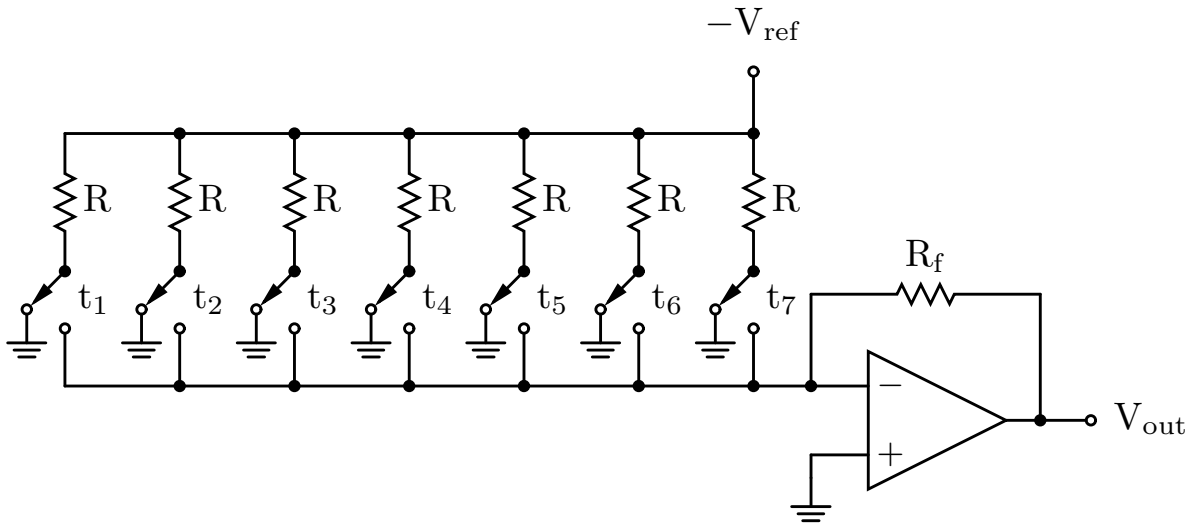
Thermometer-Code Converters

- ❏ Thermometer code: difference in one bit from next codes.
- ❏ Not a minimal representation: $2^N - 1$ bits for 2^N digital values.
- ❏ Low DNL errors: output change by only 1 LSB.
- ❏ Guaranteed monotonicity: never-lower output change.
- ❏ Reduced glitching noise:
  when the input code changes from 011 $\cdots$ 11 to 100 $\cdots$ 00.
- ❏ Same area of the analog circuitry as binary-weighted approach: since the area of resistors is proportional to their size.
- ❏ All equal-size switches since they pass equal currents.

- ❏ Thermometer codes for 3-bit binary values.

Decimal	Binary	Thermometer code
0	000	0 0 0 0 0 0 0
1	001	0 0 0 0 0 0 1
2	010	0 0 0 0 0 1 1
3	011	0 0 0 0 1 1 1
4	100	0 0 0 1 1 1 1
5	101	0 0 1 1 1 1 1
6	110	0 1 1 1 1 1 1
7	111	1 1 1 1 1 1 1
digits	$b_1b_2b_3$	$t_1t_2t_3t_4t_5t_6t_7$

❏ A 3-bit thermometer-based D/A converter.

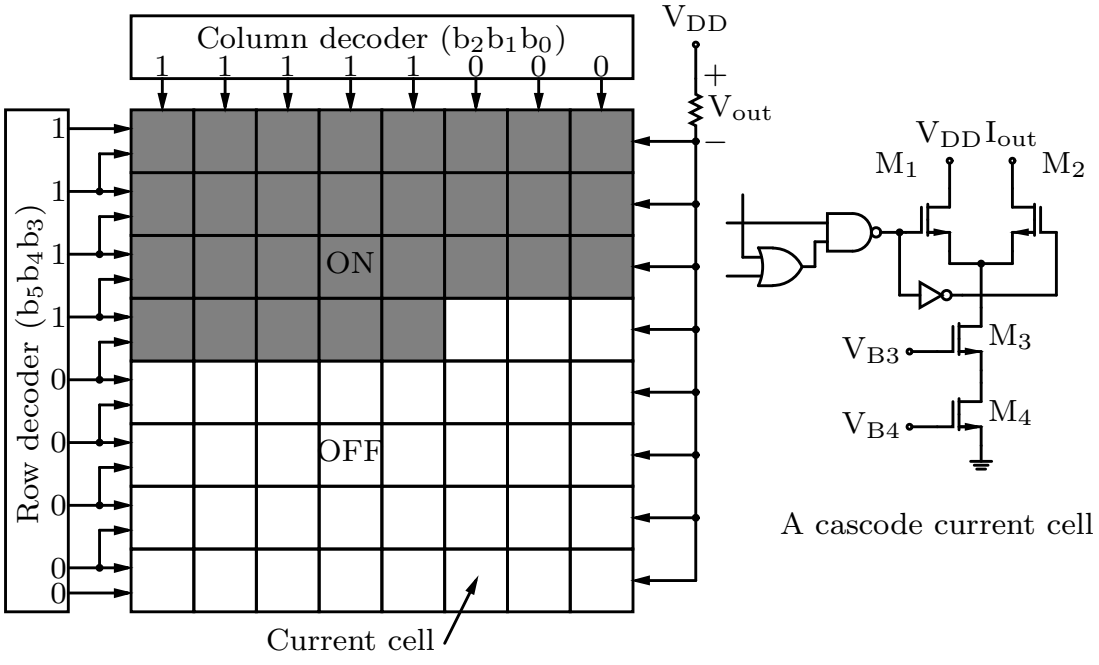


❏ A 2-bit thermometer-code charge-redistribution D/A converter.

Thermometer-Code Current-Mode Converters

- ❏ Basis for a variety of designs.
- ❏ Matrix current sources with equal value.
- ❏ Thermometer-code decoders for row and column decoding.
- ❏ Off-chip 50 Ω or 75 Ω load for high speed.
- ❏ Inherent monotonicity.
- ❏ Low DNL errors.
- ❏ Need for precise timing

- ❏ A 6-bit thermometer-code current-mode D/A converter.



A cascode current cell

Hybrid Converters

- ❏ Extremely popular approach.
- ❏ Reduced glitching and accuracy requirements in the LSBs.
- ❏ Combining the advantages of different approaches.
- ❏ Thermometer code for few MSBs + binary code for lower LSBs.
- ❏ Reduced glitching, high accuracy, saved chip area.
- ❏ Resistor-capacitor hybrid converters.
- ❏ Segmented converters.

Resistor-Capacitor Hybrid Converters

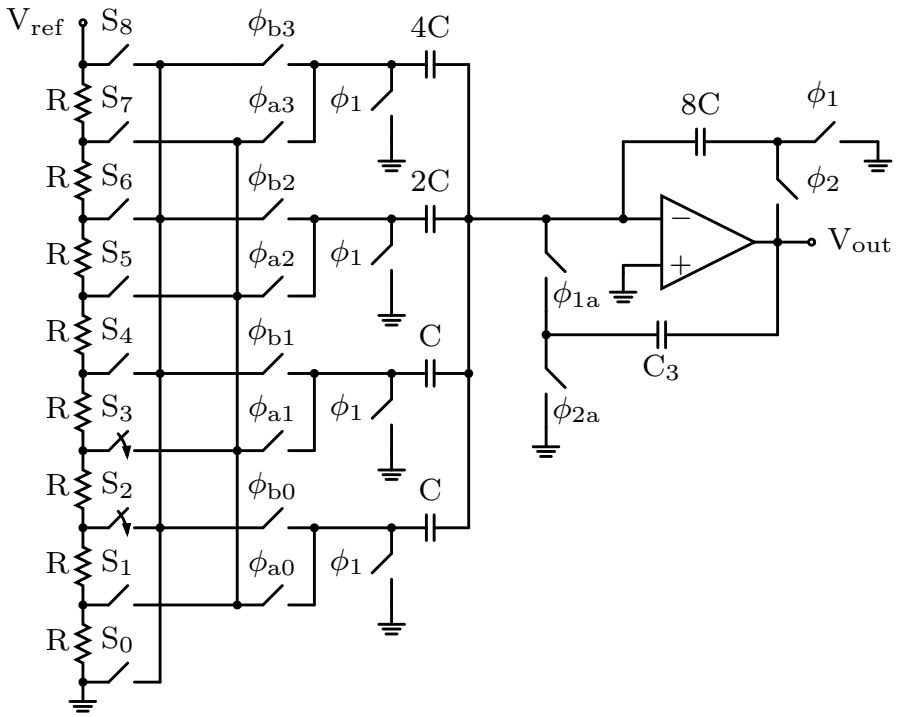
- ❏ Resistor-string DAC + SC binary-scaled DAC.
- ❏ Interpolation between the pair of voltages
  by connecting the capacitors associated with a bit 1 to the higher voltage and the capacitors associated with a bit 0 to the lower voltage.

$$V_{out} = V_i + B_{LSB}(V_{i+1} - V_i) = (1 - B_{LSB})V_i + B_{LSB}V_{i+1}$$

$$V_{out} = 2^{-3}V_i + B'_{LSB}V_i + B_{LSB}V_{i+1} \quad \text{(3-bit LSB)}$$

- ❏ 15-bit monotonicity without trimming.
- ❏ Very low power of 10 mW for 100 kHz conversion frequency.
- ❏ 3-bit resistor string + 3-bit binary-weighted PCA.

❏ A 6-bit resistor-capacitor hybrid D/A converter.



Segmented Converters

❏ The most popular design approach for D/A converters.

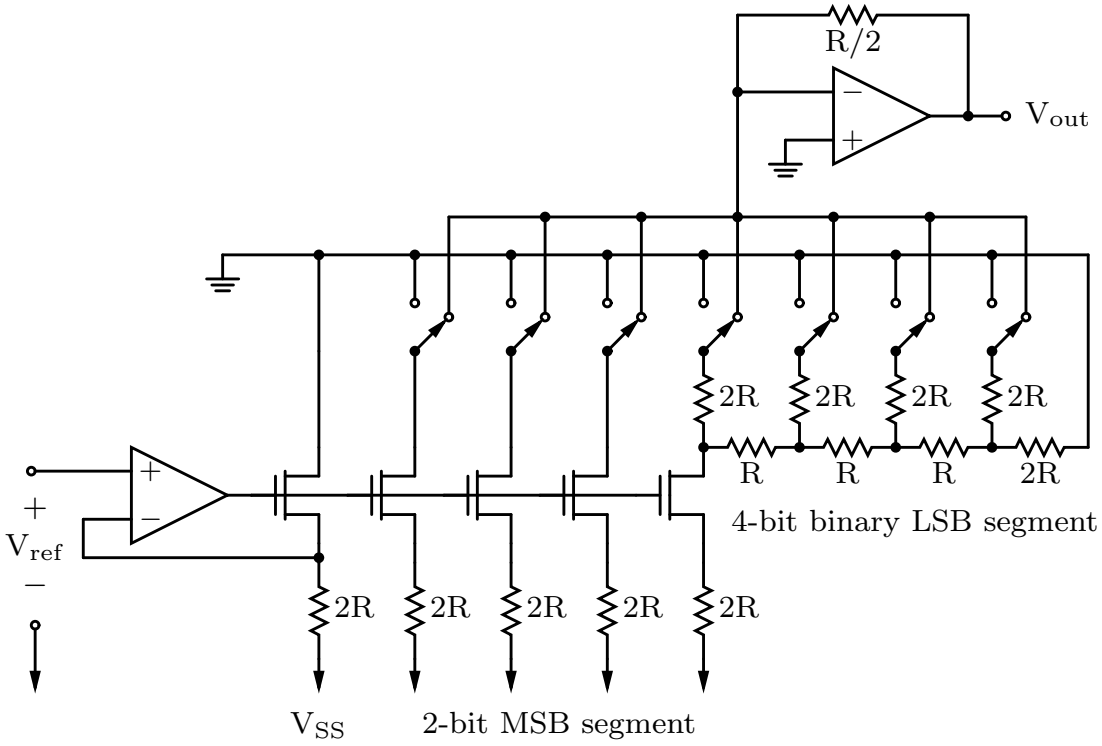
❏ Thermometer-code segment for few MSBs + binary-code segment for lower LSBs.

❏ The use of thermometer code for the MSB currents greatly minimizes glitches.

❏ One additional current source from the MSB segment is divided into binary-weighted currents of the LSB segment.

❏ Currents for high bits are switched to the output whereas low bits to ground.

❏ A 6-bit segmented D/A converter.



Homework

❏ Simulate the 2-bit binary-array charge-redistribution D/A converter. When the input code changes as follows: 00 01 10 11 10 01 00, plot the output waveform.

❏ Problems 12.2, 12.4, 12.11, 12.12, 12.17.

References

[1] Y. Nakamura, T. Miki, A. Maeda, H. Kondoh, and N. Yazawa, "A 10-b 70-MS/s CMOS D/A converter", *IEEE J. of Solid-State Circuits*, vol. 26, no. 4, pp. 637–642, 1991.

[2] A. van den Bosch, M.A.F Borremans, M.S.J. Steyaert, W. Sansen, "A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter", *IEEE J. of Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, 2001.