Data Converter Fundamentals

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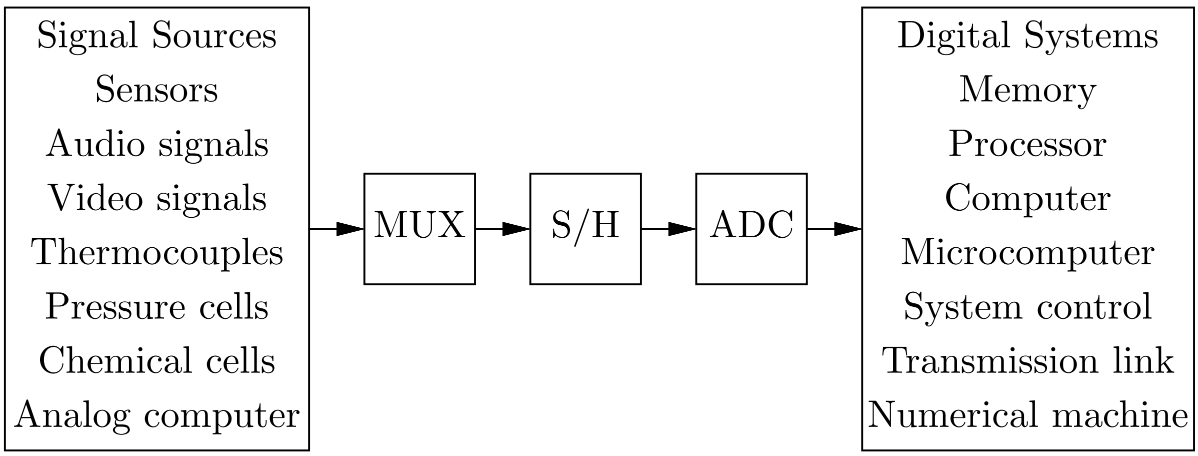
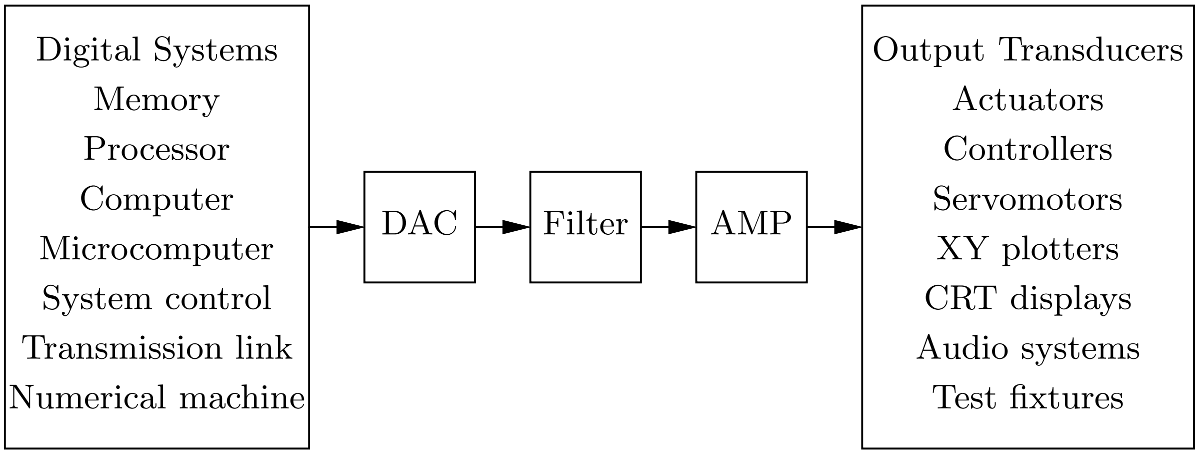
A/D Converters in Signal Processing



D/A Converters in Signal Processing

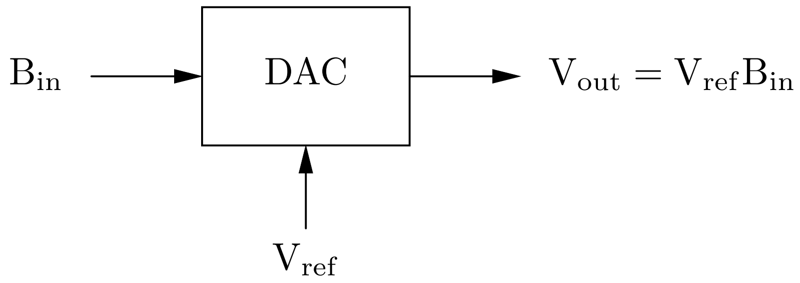


Practical Applications of Data Converters

- Camcorder
- Digital camera
- CATV, HDTV
- SVGA display, PDP
- CMOS wireless transceiver design
- Hard disk read channel

Ideal D/A Converter

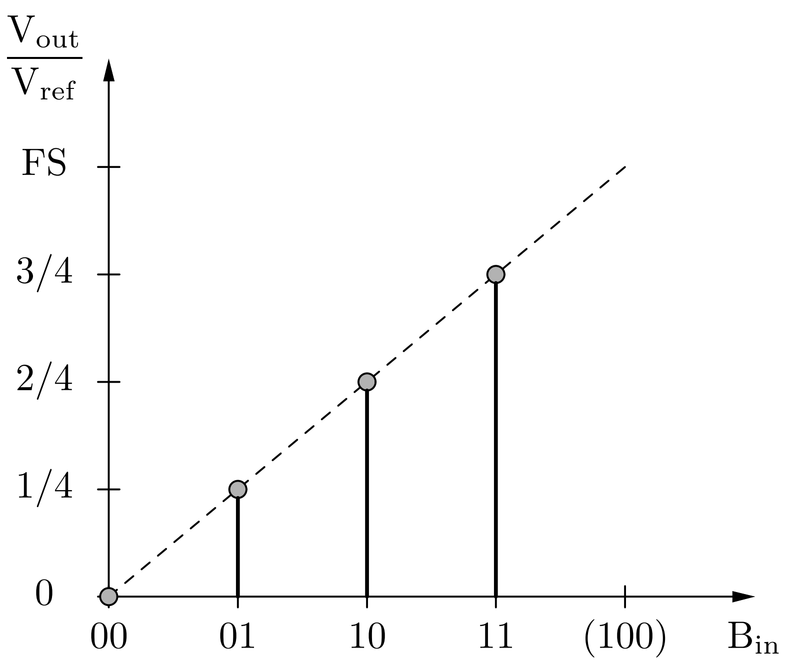
❏ N-bit D/A converter
digital signal B_{in}, reference voltage V_{ref}, analog output signal V_{out}



$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) \le V_{ref} - V_{LSB}$$

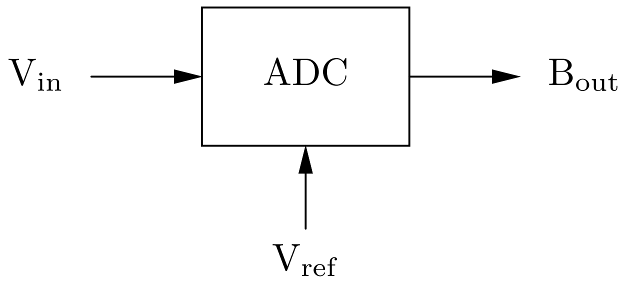
$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \qquad 1\ \mathrm{LSB} \equiv \frac{1}{2^N}$$

❏ Transfer function for an ideal 2-bit digital-to-analog converter



Ideal A/D Converter

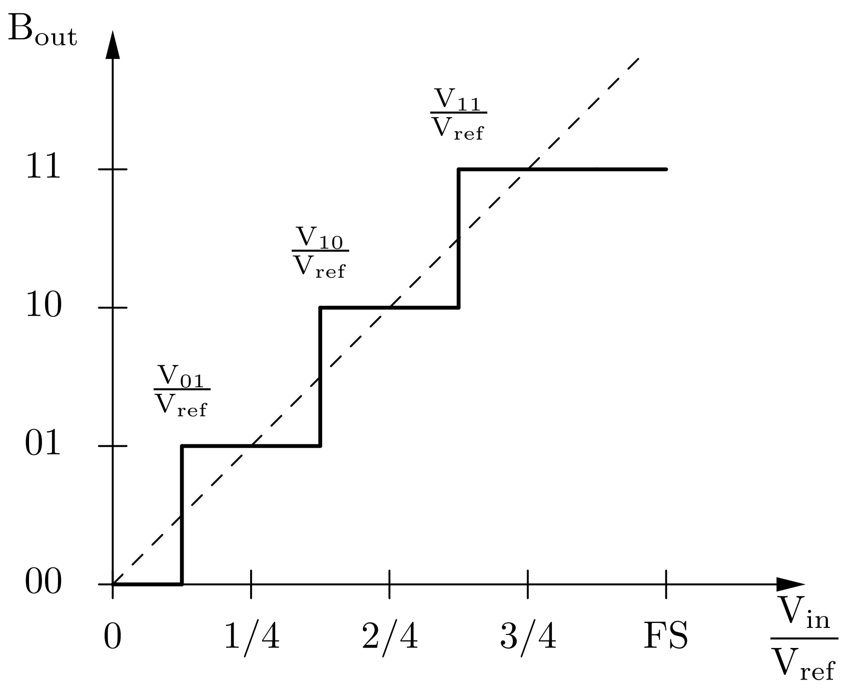
❑ N-bit A/D converter
analog input signal V_{in}, reference voltage V_{ref}, digital output B_{out}



$$V_{in} + V_Q = V_{ref}B_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N})$$

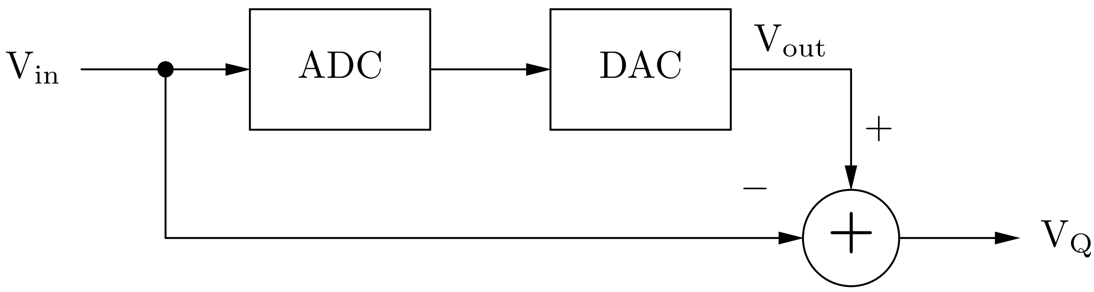
$$\text{Quantization error:} \quad -\frac{1}{2}V_{LSB} \leq V_Q < \frac{1}{2}V_{LSB}$$

❑ Transfer function for an ideal 2-bit analog-to-digital converter



Quantization Noise of Ideal A/D Converters

❑ Quantization noise: equivalent noise for quantization error

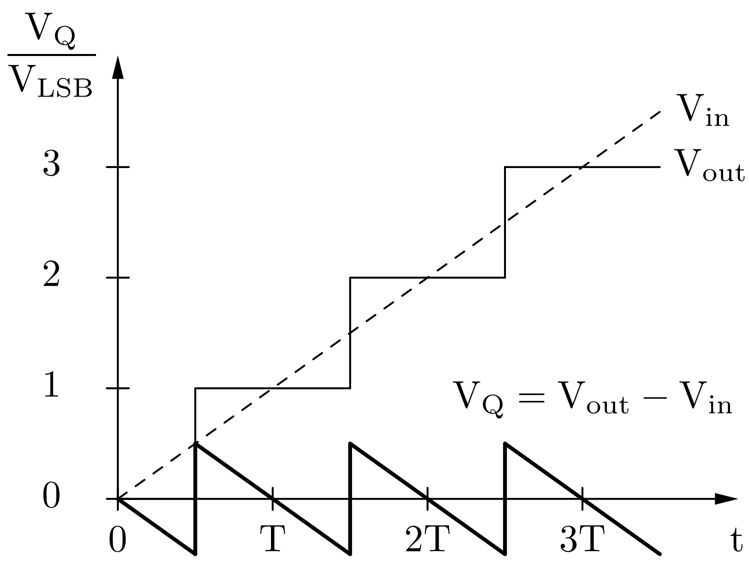


$$\text{Quantization noise} = V_Q = V_{out} - V_{in}$$

$$V_{out} = V_{in} + V_Q = \text{signal} + \text{noise}$$

❑ Deterministic approach for a ramp signal

$$V_{Q(rms)} = \left[\frac{1}{T}\int_0^T V_Q^2 dt\right]^{1/2} = \left[\frac{2}{T}\int_0^{T/2}\left(\frac{tV_{LSB}}{T}\right)^2 dt\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$



❑ Stochastic approach for a random signal

$$\text{PDF for } V_Q \;=\; f_Q(v) = \frac{1}{V_{LSB}} \quad \text{for} \quad |v| \le \frac{V_{LSB}}{2}$$

$$\text{so that} \int_{-\infty}^{\infty} f_Q(v)dv = 1 \quad \text{(normalization)}$$

$$V_{Q(avg)} = \int_{-\infty}^{\infty} v f_Q(v)dv = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} v dv = 0$$

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} v^2 f_Q(v)dv\right]^{1/2} = \left[\frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} v^2 dv\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

Deterministic approach = Stochastic approach

❑ Noise power decreases by 6.02 dB for each additional bit

Signal-to-Noise Ratio in A/D Converters

❑ Definition

$$\text{SNR} \equiv 10\log\left(\frac{\text{signal power}}{\text{noise power}}\right) = 20\log\left(\frac{V_{s(rms)}}{V_{n(rms)}}\right)$$

❑ V_{in} = sawtooth wave bounded by $\pm V_{ref}/2$

$$\text{SNR} = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log(2^N) = 6.02N \text{ dB}$$

❑ V_{in} = sinusoidal wave bounded by $\pm V_{ref}/2$

$$\text{SNR} = 20\log\left(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}}\right) = 20\log\left(2^N\sqrt{3/2}\right) = 6.02N + 1.76 \text{ dB}$$

Signed Codes for Data Converters

- Sign magnitude
  Negative number = complement of MSB for positive numbers
- 1's complement
  Negative # = complement of all the bits for positive numbers
- Offset binary
  Assigning 000 to the most negative number and then counting up as in the unipolar code

$$V_{out} \text{ of DAC} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) - 0.5V_{ref}$$

- 2's complement: subtraction is performed using addition
  Negative number = 1's complement + 1
  Complement of the MSB for offset-binary numbers

- 3-bit signed digital codes

Number	Sign magnitude	1's complement	Offset binary	2's complement
+3 = 011	011	011	111	011
+2 = 010	010	010	110	010
+1 = 001	001	001	101	001
+0 = 000	000	000	100	000
(−0)	(100)	(111)		
−1 = −001	101	110	011	111
−2 = −010	110	101	010	110
−3 = −011	111	100	001	101
−4 = −100		(011)	000	100

Performances of Data Converters

- Resolution: N-bit resolution → number of distinct analog levels
- Offset error: $V_{out}(0\cdots0) \neq 0$, $V_{0\cdots01}$ = first transition level

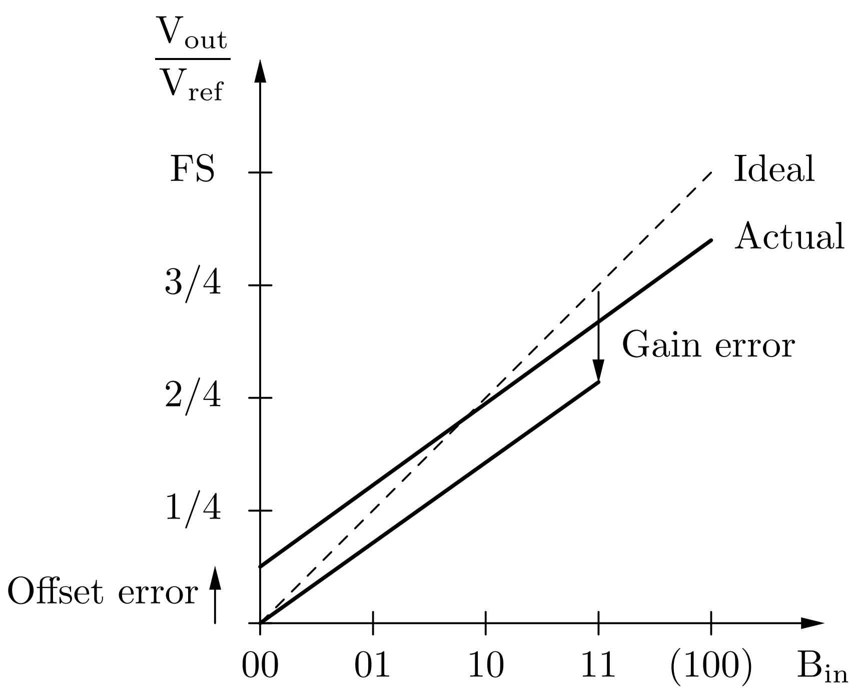
$$E_{off(D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{0\cdots0} \qquad E_{off(A/D)} = \frac{V_{0\cdots01}}{V_{LSB}} - \frac{1}{2}LSB$$

- Gain error: when $E_{off} \to 0$, $V_{1\cdots1}$ = highest transition level.

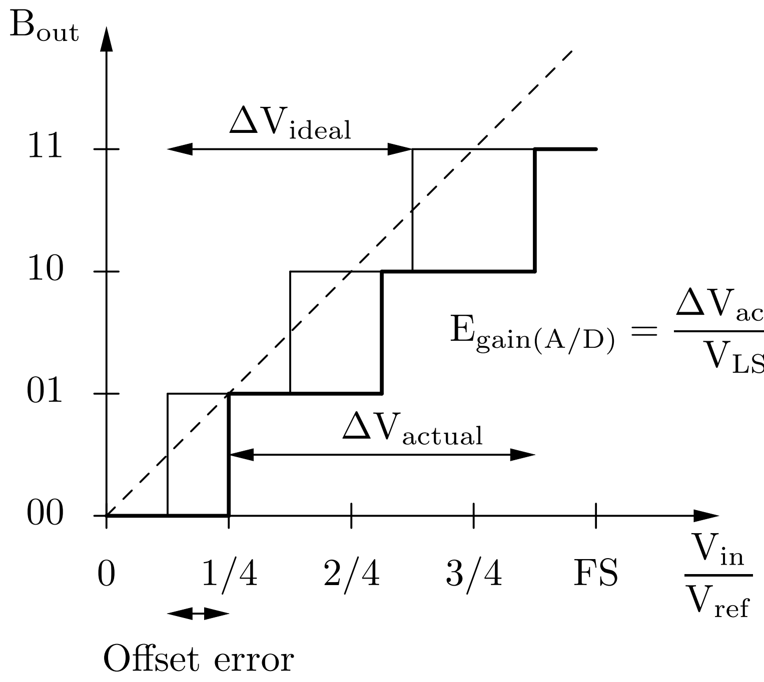
$$E_{gain(D/A)} = \left.\frac{V_{out}}{V_{LSB}}\right|_{1\cdots1} - \left.\frac{V_{out}}{V_{LSB}}\right|_{0\cdots0} - \left(2^N - 1\right)$$

$$E_{gain(A/D)} = \frac{V_{1\cdots1}}{V_{LSB}} - E_{off(A/D)} - \left(2^N - 1 - \frac{1}{2}\right)$$
$$= \frac{V_{1\cdots1}}{V_{LSB}} - \frac{V_{0\cdots01}}{V_{LSB}} - \left(2^N - 2\right)$$

- Illustration of offset and gain errors for a 2-bit DAC



❑ Illustration of offset and gain errors for a 2-bit ADC



$$E_{gain(A/D)} = \frac{\Delta V_{actual}}{V_{LSB}} - \frac{\Delta V_{ideal}}{V_{LSB}}$$

❑ Absolute accuracy
The difference between ideal and actual transfer function
⇐ offset + gain + linearity + other errors

❑ Relative accuracy = maximum integral nonlinearity error
The accuracy after offset and gain errors have been removed.

❑ Expression of accuracy
A % error of FS value, the effective number of bits (ENOB),
a fraction of an LSB

$$\mathrm{ENOB} = \frac{\mathrm{SNR} - 1.76}{6.02}$$

⇒ 10-bit resolution with 12-bit accuracy
⇒ 12-bit resolution with 10-bit accuracy

❏ Differential nonlinearity (DNL) error

The variation in analog step sizes from ideal step size (1 LSB) after the gain and offset errors have been removed.

DNLE = maximum magnitude of the DNL values in units of LSBs

❏ Integral nonlinearity (INL) error

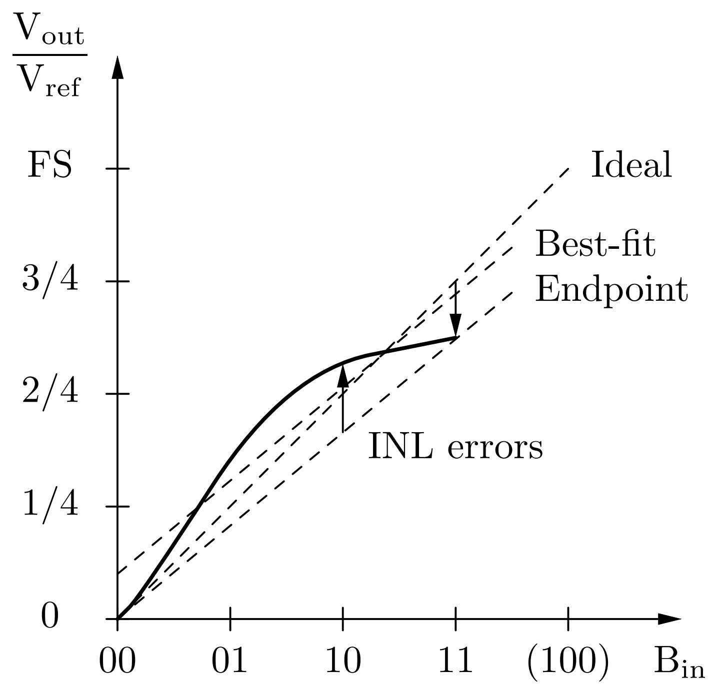
The deviation of code midpoints from a straight line after the gain and offset errors have been removed.

A straight line = ideal transfer function, endpoints, best-fit line

INLE = maximum magnitude of the INL values in units of LSBs

❏ The INL error represents the sum (integral) of the DNL errors for inputs up to the given input.

❏ Integral nonlinearity error in a 2-bit D/A converter



❏ A D/A converter transfer characteristics: $V_{ref} = 1$ V

Digital Input	Ideal DAC Output $\times V_{ref}$	A DAC Output	Step Size (LSB)	DNLE (LSB)	INLE (LSB)
000	0.0000	0.0000			0.0
001	0.1250	0.1000	0.8	−0.2	−0.2
010	0.2500	0.2500	1.2	+0.2	0.0
011	0.3750	0.3125	0.5	−0.5	−0.5
100	0.5000	0.5625	2.0	+1.0	+0.5
101	0.6250	0.6250	0.5	−0.5	0.0
110	0.7500	0.8000	1.4	+0.4	+0.4
111	0.8750	0.8750	0.6	−0.4	0.0

❏ An A/D converter transfer characteristics: $V_{ref} = 1$ V

Digital Output	Ideal ADC Transition Point $\times V_{ref}$	An ADC Transition Point	Step Size (LSB)	DNLE (LSB)	INLE (LSB)
000					
001	0.0625	0.0625	0.5	0.0	0.0
010	0.1875	0.2500	1.5	+0.5	+0.5
011	0.3125	0.3125	0.5	−0.5	0.0
100	0.4375	0.4375	1.0	0.0	0.0
101	0.5625	0.5625	1.0	0.0	0.0
110	0.6875	0.7500	1.5	+0.5	+0.5
111	0.8125	0.8125	0.5	−0.5	0.0

❑ Monotonicity for DACs
The slope of transfer function > 0
$\Leftarrow$ DNLE < 1 LSB or INLE < 0.5 LSB

❑ Missing codes for ADCs
The ability to correspond all possible digital codes to an analog input
$\Leftarrow$ DNLE < 1 LSB or INLE < 0.5 LSB

❑ A/D conversion time and sampling rate
The time taken to complete a single conversion including acquisition time of the input signal (multiplexing).

$$\text{Sampling rate} \leq \frac{1}{\text{Conversion time}}$$

❑ D/A settling time and conversion rate
The time taken to settle to within some specified amount (usually 0.5 LSB) of the final value.

$$\text{Conversion rate} \leq \frac{1}{\text{Settling time}}$$

❑ Sampling-time uncertainty = aperture jitter
For sinusoidal waveforms,

$$v = \frac{V_{ref}}{2}\sin(2\pi f t), \qquad \left.\frac{\Delta v}{\Delta t}\right|_{max} = \pi f V_{ref}$$

During some sampling-time uncertainty, to keep $\Delta v < V_{LSB}$

$$\text{Aperture jitter } \Delta t < \frac{V_{LSB}}{\pi f V_{ref}} = \frac{1}{2^N \pi f}$$

- Dynamic range

  The ratio of the rms value of maximum amplitude input sinusoidal signal to the rms output noise plus distortion (SNDR).

  The rms output noise plus distortion is obtained by eliminating the sinusoid from the measured output. For a D/A converter, the output sinusoid can be eliminated by using a spectrum analyzer. For an A/D converter, a similar approach can be taken by using FFT.

  The dynamic range may be a function of the frequency of the sinusoidal input and the input signal level. The dynamic range can be expressed as an effective number of bits (ENOB).

$$\mathrm{SNDR} = 6.02\mathrm{N_{eff}} + 1.76$$

  Example: fundamental power = 1 W, remaining power = 0.5 μW

$$\mathrm{SNDR} = 10\log(1/0.5\mu) = 63\ \mathrm{dB},\ \ \mathrm{N_{eff}} = (63 - 1.76)/6.02 = 10.2\ \mathrm{bits}$$

Homework

- Problems 11.2, 11.3, 11.7, 11.8, 11.12